Letter _____

Active-Forced-Commutated Bridge Using Hybrid Devices for High Efficiency Voltage Source Converters

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***Abstract*—In high power converters, the on-state characteristics of semiconductor devices dictate its efficiency performance even if the optimized topologies are adopted. This letter proposes an active-forced-commutated (AFC) bridge that employs the hybrid power devices of thyristor and insulated-gate bipolar transistor (IGBT) to operate as a voltage source converter (VSC) or the building blocks of complex multi-stage high-voltage high-power converters. In this scheme, the thyristors are placed in the main power path that conducts for most of the fundamental period to lower the on-state losses; while the IGBT based full-bridge chain-link (FB-CL) is used for controlled (soft) transition and forced commutation of the main thyristor bridge, operating in short period. This stepped transition voltage also leads to minimized *dv/dt* exerted on the interfacing transformer. To coordinate the operation of these two parts, the FB stack is designed to operate in a concave polygon stepped transition (CPST) mode for the ordered turn-on and turn-off of thyristors according to different categories of commutation events. Detailed commutation analysis for the AFC-bridge is provided in this letter; also, high level discussions and simulation results are presented to demonstrate its potential technical merits.**

***Index Terms*—Voltage source converter (VSC), hybrid device, thyristor, IGBT, high efficiency, controlled transition, active-forced-commutation (AFC).**

I. Introduction

High capacity high efficiency voltage source converters (VSCs) are the enabling technology for driving the realization of generic multi-terminal high voltage direct current (HVDC) transmission networks. VSC based HVDC can address the weaknesses of using the conventional line commutated converter (LCC), namely the commutation failure under weak ac networks, high reactive power consumption and limited control flexibility. Thus, VSC has extended the role of HVDC into applications requiring flexible terminal voltage control, weak ac grid compatibility, rapid power flow reversal (without reversing the dc-link voltage polarity as in LCC), and multi-terminal configuration [1, 2].

VSC topologies for HVDC applications have evolved from the two-level and monolithic multilevel converters to the modular multilevel converter (MMC) and its variants. Current MMC topologies are able to achieve true voltage scalability, system redundancy and internal fault management. Also, the use of multilevel modulation leads to reduced switching losses and d*v*/d*t* exerted on the transformers [3, 4].

Despite the stated benefits of VSC-HVDC, thyristor based LCC-HVDC has maintained advantages in terms of capacity and efficiency; thus, it remains dominant in the large power evacuation through ultra-high voltage direct current (UHVDC) links. These advantages result from the use of high capacity thyristors with extremely low on-state losses. For example, the 4.5kV/1.8kA insulated-gate bipolar transistor (IGBT) module T1800GB45A has a typical forward voltage of 3.7V; while the on-state voltage of 4.8kV/1.77kA thyristor T1551N48TOH is 1.57V~1.7V. Several hybrid configurations of LCC and MMC have been put forward in attempt to achieve a trade-off between efficiency and operational flexibility [5-7]. However, the current source nature of LCC in above solutions requires dc-link voltage reversal to change the power flow direction, reducing the compatibility with other VSC terminals in multi-terminal HVDC networks.

This letter proposes the active-forced-commutated (AFC) bridge using hybrid switching devices (thyristor and IGBT) to operate as a VSC or basic building block of a complex UHVDC power converters. It employs thyristors to transfer the main power efficiently; while an IGBT based full-bridge chain-link (FB-CL) is used to actively control the turn-on and turn-off of the main thyristor-bridge by applying a stepped transition voltage with appropriate magnitude and polarity, which offers soft switching and forced commutation to the thyristors. In this manner, the VSC nature is established for the AFC-bridge; thus, the active and reactive power control can be decoupled. Compared to LCC, this solution enables the thyristor operation free of ac grid strength. Moreover, it offers dc-fault blocking capability and power flow reversal either with or without changing the dc-link voltage polarity, which is similar as the full-bridge MMC in terms of functionality but at much lower losses. The AFC-bridge is expect to unlock the possibility of using VSC in UHVDC link (±800kV or beyond) with similar efficiency of LCC. To ensure proper operation, the FB-CL of the proposed converter works in a concave polygon stepped transition (CPST) mode; also, it can act as the backup free-wheeling path during current sampling mismatch or when the load current level is below the thyristor latching current. Operation principle and modulation strategy of the AFC-bridge is provided in the letter.

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II. Proposed Active-Forced-Commutated Bridge

A. Operational Principle of the AFC-Bridge

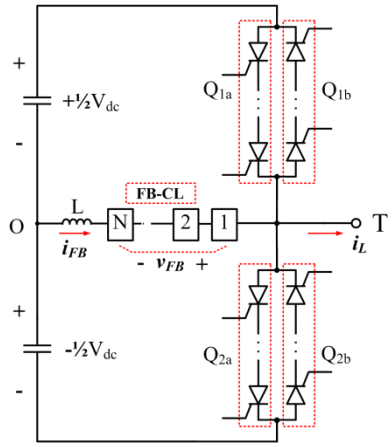

Fig. 1. Proposed AFC-bridge using hybrid power devices.

The configuration of the proposed AFC-bridge is depicted in Fig. 1, where series connected thyristors Q_{1a} and Q_{2a} are employed as the main power switches with anti-parallel thyristor strings Q_{1b} and Q_{2b} as current freewheeling paths for full power factor range. The commutation of thyristor-bridge is guaranteed by the actively controlled FB-CL that provides reversible voltage to force the thyristors to turn off. This auxiliary FB-CL is a string of FB modules using the self-commutated IGBT, which is active only during thyristor commutation. Therefore, its average power dissipation is low and the associated cooling system is small, without significant impact on the overall efficiency and power density.

To ensure the ordered turn-on and turn-off of thyristors, one thyristor is fired at each instance based on the voltage level command and current polarity, and the FB-CL acts as the free-wheeling path when the load current is below the thyristor latching current or during any current sampling mismatch. In Fig. 1, if the AFC-bridge dc-link voltage is V_{dc} with neutral point O, the FB-CL should be designed to have internal redundancy that allows the trajectory of its output voltage v_{FB} to go beyond the envelopes of $\pm½V_{dc}$. When v_{FB} is higher (lower) than $+½V_{dc}$ ($-½V_{dc}$), the upper (lower) thyristor string Q_{1a} (Q_{2a}) can be turned-off provided its gate signal is removed. In another side, the turn-off of anti-parallel devices Q_{1b} (Q_{2b}) can be realized when v_{FB} is lower (higher) than $+½V_{dc}$ ($-½V_{dc}$). Also, the FB-CL offers stepped transition and zero-voltage-switching (ZVS) for the thyristor to be compatible with the critical dv/dt and di/dt for device safe operation.

Over the majority of the operation period (thyristor conduction status), the FB-CL sustains a voltage of $\pm½V_{dc}$. To block this voltage, if V_U is the capacitor voltage on each FB unit, N_T of them should be inserted into the FB-CL path; thus, (1) can be obtained. Also, a group of redundant FB modules are required in the FB-CL to supply a maximum output voltage larger than $½V_{dc}$ by V_C. Suppose N_C FB units are employed to generate this additional voltage V_C as in (2); therefore, the total number of FB units in the FB-CL N is obtained by (3).

$$N_T \cdot V_U = ½V_{dc} \quad (1)$$

$$N_C \cdot V_U = V_C \quad (2)$$

$$N = N_T + N_C \quad (3)$$

The AFC-bridge achieves dc-fault blocking capability by inhibiting the gate signals from both thyristors and IGBTs of the FB-CL. In this manner, the total FB-CL capacitor voltage can effectively decay the dc fault current.

B. AFC-Bridge Commutation With FB-CL in CPST Mode

As analyzed previously, when load current i_L is positive, commutation happens between the upper main thyristor (Q_{1a}) and the lower anti-parallel device (Q_{2b}) with other thyristors turned off; while if i_L is negative, Q_{1b} and Q_{2a} will participate in the voltage level transition. For symmetry, Fig. 2 interprets the commutation process of the AFC-bridge by assuming i_L in positive direction. As in Fig. 2, the FB-CL is modulated in a CPST mode with its voltage and current noted as v_{FB} and i_{FB}, respectively; which is able to control the voltage and current waveforms of Q_{1a} and Q_{2b}. The full commutation process is shown in Fig. 2, where, for clear demonstration, the transition period is expanded relative to the conduction state. Detailed explanations for each stage of Fig. 2 are as follows:

- [t_0-t_1]: initially, both Q_{1a} and Q_{2b} are turned off; while the FB-CL current i_{FB} supply the load current; thus, with the current direction definition in Fig. 1, we have $i_{FB}=i_L$ and $v_{TO}=v_{FB}$.
- [t_1-t_2]: with the increase of v_{FB} to $+½V_{dc}$, the voltage of Q_{1a} decreases to zero. Then, Q_{1a} is triggered and N_C units of the FB-CL are blocked (with blocking voltage V_C), making the output current commutate from the FB-CL to Q_{1a} under ZVS turn-on. In this period, the lower thyristors Q_{2a} and Q_{2b} sustain the voltage of $+V_{dc}$.
- [t_2-t_3]: the FB-CL current reduces to zero; and the full current flows through the thyristor Q_{1a}. This period is used for main power transfer and the AFC-bridge generates $+½V_{dc}$ on converter pole T relative to the dc neutral point O.
- [t_3-t_4]: with the voltage level transition command, the Q_{1a} gate signal is removed and the FB-CL voltage v_{FB} increase to $½V_{dc}+V_C$ by its redundant FB modules, facilitating a negative net voltage of $-V_C$ across the Q_{1a} conduction loop (since Q_{1b} is not triggered), which forces the Q_{1a} current to decrease. At the same time, i_{FB} rises in order to support the full load current.
- [t_4-t_5]: at t_4, the Q_{1a} current decreases to negative peak value, establishing the required reverse bias voltage. After its reverse recovery process, a voltage of $-V_C$ on Q_{1a} and Q_{1b} lasts until t_5 with the load current fully transferred to the FB-CL. Q_{2a} and Q_{2b} block the voltage of $V_{dc}+V_C$.
- [t_5-t_6]: since Q_{1a} has been forced turned-off, the FB-CL voltage v_{FB} starts to decrease from $½V_{dc}+V_C$ to $-½V_{dc}$ in a stepped transition manner, which offers the soft transitions to the thyristors.

- [t_6-t_7]: at t_6, the blocking voltage of V_{dc} is established on Q_{1a} and Q_{1b}; while the voltage on Q_{2a} and Q_{2b} becomes zero. With Q_{2b} being triggered and the N_C FB modules being disabled, the output current transits from the FB-CL to Q_{2b} in ZVS turn-on manner.

Then, Q_{2b} carries the full load current during t_7-t_8 and the similar forced commutation and stepped transition processes are performed by the FB-CL to execute the voltage level transition command. After t_{10}, the initial state in t_0-t_1 starts and the same processes are repeated for positive i_L.

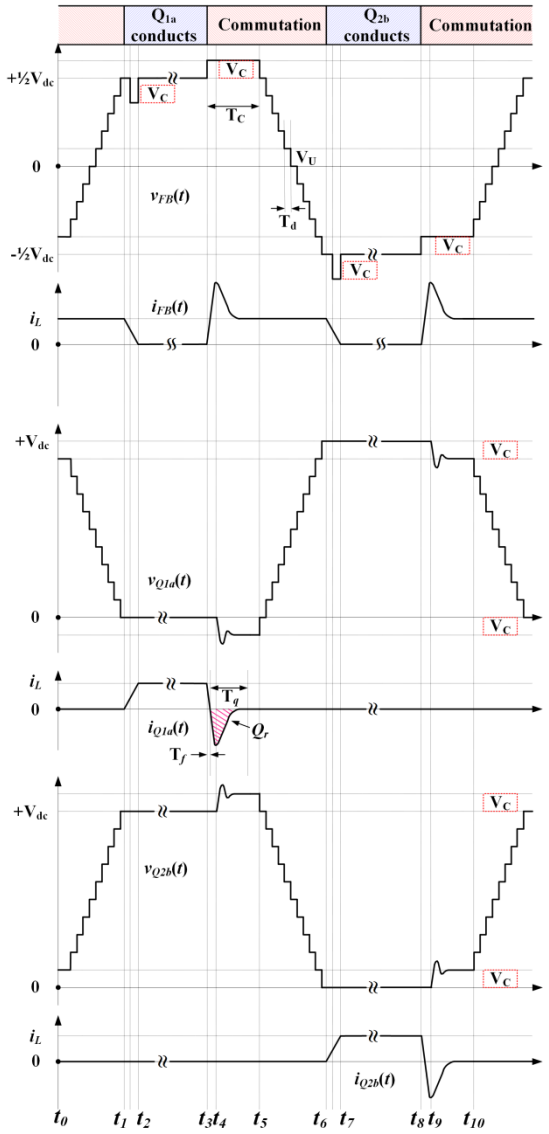

Fig. 2. Commutation of the AFC-bridge (when load current i_L>0) with FB-CL operating in CPST mode.

It is noticed that the principal power is transferred through the low loss thyristors during intervals of t_2-t_3 and t_7-t_8 that form the majority of the operation period; also, the switching losses are minor due to the stepped transition of the FB-CL. When i_L is in negative direction, the symmetrical process of Fig. 2 will apply to the FB-CL, Q_{1b} and Q_{2a}. The voltage balancing of FB-CL sub-modules can be realized using its redundant switching states to charge or discharge the selected capacitors based on the sorting results [8].

C. *Current Natural Commutation Event Management*

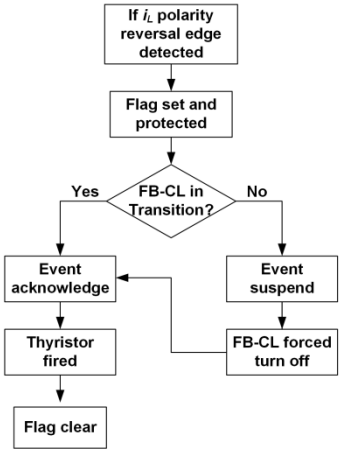

Fig. 3. Response to the current natural commutation event.

To guarantee the causal, ordered and reliable operation of the AFC-bridge, only one thyristor is fired at each instance based on the voltage level command and current polarity; and it must be forced turned off by the FB-CL before the gate signal moving to next device. During this period, the FB-CL is able to serve as the free-wheeling path for current sampling mismatch and zero-crossing current lower than the thyristor latching current. In order to minimize the free-wheeling time of FB-CL, the current natural commutation (zero-crossing) events should be managed as in Fig. 3, where two categories of event triggers are responded by the AFC-bridge as follows.

If current zero-crossing is detected during the voltage level transitions, the event will be acknowledged directly; and after the FB-CL is disabled, the proper thyristor for conducting the reversed current flow will be fired. While if the current zero-crossing happens out of the voltage level transition periods, the FB-CL is utilized to force the previous thyristor to turn-off; then its anti-parallel device will be fired to carry the reversed current. This regime ensures any previously triggered thyristor must be turned off by the FB-CL before next thyristor is turned on and the FB-CL itself provides a free-wheeling path for seamless current operation. As a result, the ordered and causal commutation of the AFC-bridge can be facilitated.

D. *Converter Dimensioning Guidelines*

From Fig. 2, the total charge required for forced turned-off of the thyristor can be estimated by the integration of the output current (i_L) over the thyristor negative voltage duration T_c plus the thyristor recovered charge Q_r, which is expressed by (4). For a given allowable voltage ripple percentage of κ on the FB capacitors, the FB unit capacitance C_U is determined by (5), where κ should satisfy the inequality of (6) to ensure that the total capacitor voltage of the FB-CL remains greater than ½V_{dc}. After the thyristor is turned off, the FB-CL conducts the load current i_L and provides an orderly transition with short dwelling time T_d (T_d<<T_C) at each voltage step. For a sinusoidal output current i_L and based on (4)-(5), the FB unit capacitance can be calculated by (7).

$$Q_C = \int_{t_i}^{t_i+T_C} i_L(t)\cdot dt + Q_r \tag{4}$$

$$Q_C = \kappa(\tfrac{1}{2}V_{dc} + V_C)\cdot\frac{C_U}{N} = \kappa V_U \cdot C_U \tag{5}$$

$$\kappa < V_C / (\tfrac{1}{2}V_{dc} + V_C) \tag{6}$$

$$C_U = \frac{1}{\kappa V_U}\left[\int_{\omega-\frac{1}{2}T_C}^{\omega+\frac{1}{2}T_C} I_{ac}\cos(\omega t-\theta)\cdot dt + Q_r\right] = \frac{I_{ac}T_C\cdot\mathrm{sinc}(\frac{1}{2}\omega T_C)+Q_r}{\kappa V_U} \tag{7}$$

The FB-CL branch inductance L determines the di_{FB}/dt during the thyristors turn-on and turn-off. It must be sized such that the maximum permitted current ramp rate ζ of the adopted thyristors is not exceeded. Also, to ensure reliable turn-off of the thyristor, the reverse bias time T_C should be larger than device turn-off time T_q; and the current falling time T_f must be shorter than T_C–T_q. Therefore, the constraints for calculating L can be summarized as in (8).

$$\frac{i_L}{T_C - T_q} \le \frac{V_C}{L} \le \zeta \tag{8}$$

III. Performance Evaluation and Discussion

The AFC-bridge is possible to operate as an independent VSC or the building blocks of many other converters such as the front-to-front (F2F) dc-dc converter, dc auto-transformer (AT) and MMC, see Fig. 4 [9, 10].

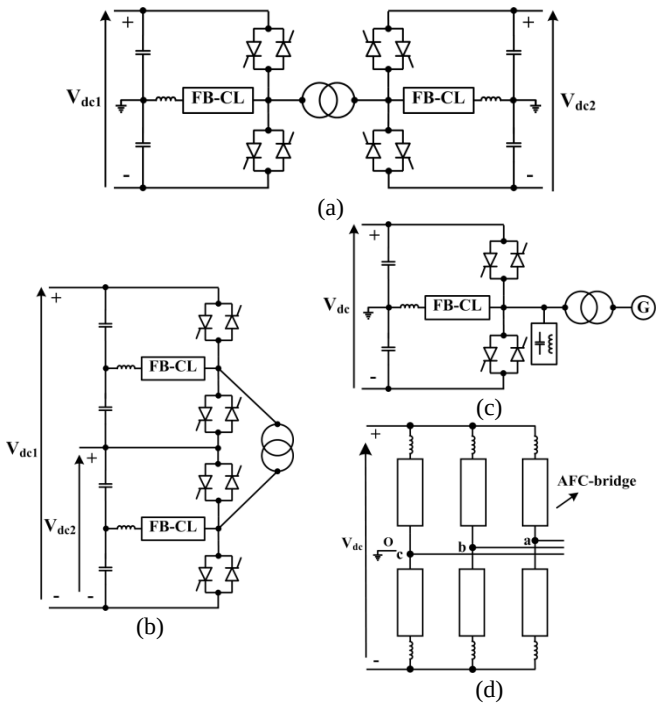

Fig. 4. AFC-bridge applied in HVDC transmission system: (a) F2F dc-dc converter; (b) dc-dc AT; (c) dc-ac converter; (d) MMC arm.

In dc-dc applications, the AFC-bridge could be operated with trapezoidal waveform. The FB-CL is used to generate the slope for soft transition of the main thyristor devices; while the majority of the power is transferred through the thyristors. Due to the high operational power factors of the AFC-bridge in its dc transformer configuration, the anti-parallel thyristors can be low current rated.

If the AFC-bridge operates as a dc-ac converter or needs to supply black-start capability in a dc transformer, the dc-rail clamping period, zero-voltage level duration and voltage level transition slope of its ac voltage waveform can be manipulated to vary the modulation index in full range. In these cases, the FB-CL may operate longer period for better voltage wave quality but with limited sacrifice of converter efficiency. The triplen harmonic injection could be used to further extend the modulation range of the AFC converter [8, 11]. An alternative option is to use the selective harmonic elimination (SHE). However, the number of switching angles is limited by the thyristor commutation speed. The tuned-filters are required to eliminate low order harmonics for ac grid connection.

For a generic verification of the AFC-bridge commutation, SHE with one switching angel per quarter cycle is employed for a simulation study. The specifications are as follows: dc-link voltage: 150kV; FB cell capacitor: 5mF, FB number: N=11, N_T=10, N_C=1; FB-CL inductance: 750μH, three-phase power rating: 160MVA, ac side peak phase current: 1.5kA.

The zoomed-in version of the thyristor forced turn-off in the AFC-bridge is shown in Fig. 5, where the upper main thyristor Q_{1a} and lower anti-parallel thyristor Q_{2b} both have forced commutation and voltage level stepped transition processes offered by the FB-CL as in Fig. 2. It is noticed that, to save simulation time, the reverse recovery of thyristor is not modeled in this case study. Since this process finishes within the forced turn-off period, it will not influence the presented modulation scheme.

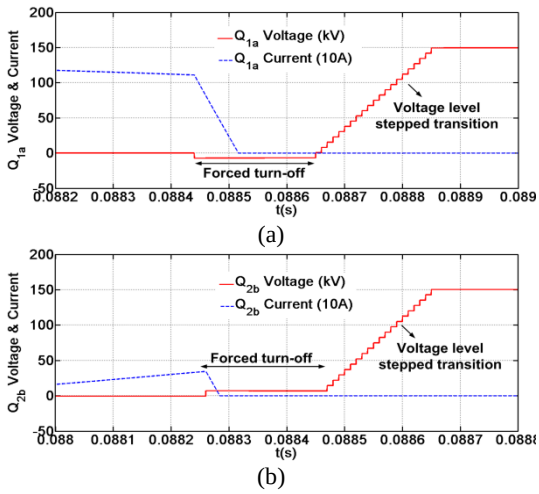

Fig. 5. Zoomed-in switching waveforms for thyristors in the AFC-bridge: (a) turn-off and stepped transition of Q_{1a}; (b) turn-off and stepped transition of Q_{2b}.

The key waveforms of the AFC-bridge in fundamental time scale are summarized in Fig. 6. The output voltage with one switching angle per quarter cycle and output current with 1.5kA peak value are shown by Fig. 6(a). Observe in Fig. 6(b), the FB module capacitor voltages can be kept balanced by the redundant switching states of the AFC-bridge. According to Fig. 6(c), the FB-CL only conducts during short periods of thyristor commutation and load current zero-crossing; also, by utilizing the blocking states of the FB-CL, its current decays naturally and the load current can be smoothly routed into the

thyristor. In this way, the majority of load current is carried by the main thyristors Q_{1a} and Q_{2a} alternatively in this high power factor case as in Fig. 6(d); and their anti-parallel devices are exposed to low currents. When power factor decreases, the current distribution in anti-parallel thyristors will increase.

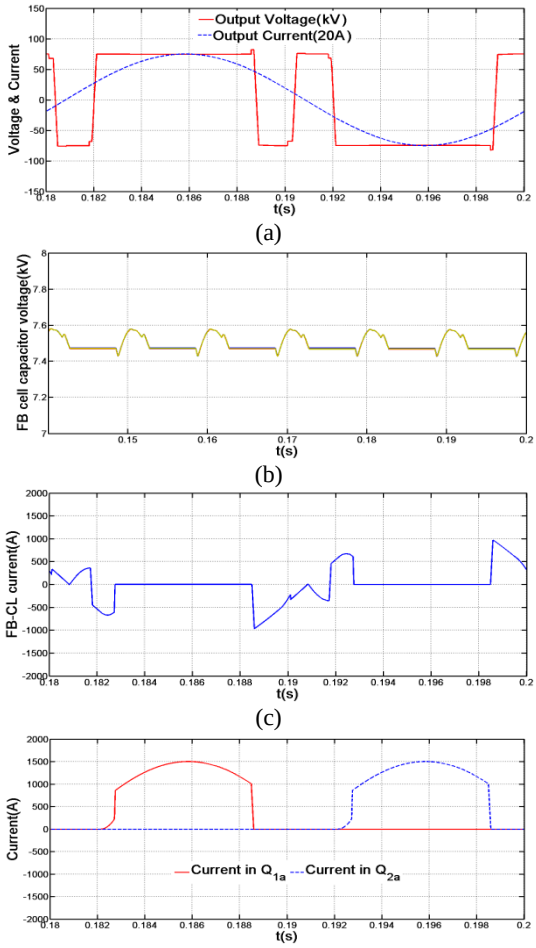

Fig. 6. Key waveforms of the AFC-bridge: (a) output voltage and current; (b) FB capacitor voltage balancing; (c) FB-CL current; (d) current carried by thyristor Q_{1a} and Q_{2a}.

IV. Conclusions

This letter has proposed an active-forced-commutated (AFC) bridge with hybrid devices of thyristors and IGBT for high efficiency HVDC converters. Instead of having live ac grid voltage as prerequisite for successful line commutation of the thyristors in LCC, the AFC-bridge employs its full-bridge chain-link (FB-CL) circuit to offer soft transition and forced commutation to the thyristors. In this manner, their fully controlled turn-on and turn-off are realized, which allows the AFC-bridge to operate the thyristors as a VSC with weak ac grid compatibility under full power factor range and black-start capability from a given dc-link voltage. Furthermore, by using the symmetrical thyristors as main power paths, the AFC-bridge has even lower semiconductor losses than the half-bridge MMC, but offers equivalent system functionalities as the full-bridge cell MMC. These functions such as the dc fault blocking, continuous operation under reduced dc-link voltage as well as bipolar dc-link voltage and bidirectional current capability ensure its coordination with both VSC and LCC terminals. The proposed AFC-bridge is highly applicable in HVDC systems such as front-to-front (F2F) dc-dc converter and dc-dc auto-transformer (AT); while in its dc-ac scenarios, a group of tuned-filters are necessary to remove the dominant low order harmonics.

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