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Stencil-HMLS: A multi-layered approach to the automatic optimisation of stencil codes on FPGA

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ABSTRACT
The challenges associated with effectively programming FPGAs have been a major blocker in popularising reconfigurable architectures for HPC workloads. However new compiler technologies, such as MLIR, are providing new capabilities which potentially deliver the ability to extract domain specific information and drive automatic structuring of codes for FPGAs.

In this paper we explore domain specific optimisations for stencils, a fundamental access pattern in scientific computing, to obtain high performance on FPGAs via automated code structuring. We propose Stencil-HMLS, a multi-layered approach to automatic optimisation of stencil codes and introduce the HLS dialect, which brings FPGAs programming into the MLIR ecosystem. Using the PSyclone Fortran DSL, we demonstrate an improvement of $14-100\times$ with respect to the next best performant state-of-the-art tool. Furthermore, our approach is $14-92\times$ more energy efficient than the next most energy efficient approach.

KEYWORDS
FPGAs, U280, MLIR, xDSL, HPC, stencil based codes

1 INTRODUCTION
Programming FPGAs is hard, and it is even more difficult to program these effectively to exploit the full potential of the hardware. Arguably this is one the main reasons that the technology has not become more commonplace in our supercomputers. As the supercomputing community continues to progress into the exascale era, and our HPC machines become more heterogeneous, it is not realistic to expect scientific programmers to be able to master all these complex, architecture specific, performance optimisation techniques. One solution is that of Domain Specific Languages (DSLs), which are high-level abstractions that provide a richness of expressivity which enables the scientific end users to express their problem in a manner that is far closer to their domain of expertise. The term language is somewhat of a misnomer as instead it has become popular for DSLs to provide abstractions within existing programming languages that provide an interface for expressing a rich amount of information about the problem that can be passed down the compiler stack for the tooling to make informed, automatic, decisions around optimisation.

Being able to effectively exploit FPGAs for high performance workloads is a prime example of where a DSL is potentially helpful. Whilst there are numerous studies of HPC applications on FPGAs, these involve significant manual optimisation of the code. Not only is this a time consuming process that requires significant FPGA expertise from the programmer, but furthermore the resulting code is often very different from its CPU or GPU counterpart. An example of this type of problem is with stencil-based kernels, which underlie many scientific codes. Stencils are ubiquitous in HPC applications, and whilst there have been numerous studies exploring the techniques required in gaining optimal performance on FPGAs, it is not realistic to expect scientific programmers to be able to master these.

In this paper we use PSyclone, which is a Fortran based DSL for weather and climate simulations, as a vehicle to explore our approach in driving automatic optimisations of classes of HPC algorithms via MLIR for FPGAs. Focusing on stencil-based codes due to their ubiquity, we propose Stencil-HMLS (High-Multi Level Synthesis), a framework for automatic optimisation of stencil codes. Hence the contributions of this paper are as follows:

1. A new HLS MLIR dialect which abstracts dataflow concepts on FPGAs and is able to then be lowered directly to AMD Xilinx’s HLS backend.
2. Transformations from the existing MLIR stencil dialect to our HLS dialect, demonstrating that one can leverage the rich amount of domain specific information to apply dataflow specific optimisations.
3. Demonstration of how MLIR can be integrated with DSLs such as PSyclone to target FPGAs in a manner that requires little effort on behalf of the DSL developer.

The rest of this paper is structured as follows: Section 2 provides an outline of the related work and establishes comparison points with our work that we will pick on on the evaluation, Section 3 describes the implementation of the HLS dialect and the transformations that enable the automatic optimisation of stencils on FPGAs, Section 4 presents the results that assess the performance of...
2 BACKGROUND AND RELATED WORK

2.1 Auto-optimisation of codes for FPGAs

There have been several efforts to synthesise Von-Neumann based codes which were not designed for dataflow architectures into a form that will deliver good performance on FPGAs. Some approaches, such as DaCe [3], advocate performance portability, where the framework compiles codes into a dataflow IR, that they call Stateful Dataflow MultiGraph (SDFG), and this is then lowered to CPU, GPU or FPGA targets. DaCe is interesting because it seeks to decouple the responsibilities of the domain scientist from the performance specialist, where the first can focus on their domain of mathematics using Python that is then lowered into an SDFG representation which can be optimised either manually by the performance engineer or automatically by the tooling. In order to achieve good results, however, this approach requires either manual construction of the SDFG or significant optimisation by the performance expert of the generated SDFG.

The StencilFlow [8] tool has been built atop DaCE as it generates SDFGs for stencil based kernels based upon a JSON description. Although it is possible to generate the JSON description automatically, this is highly code specific and there is no general way in which the JSON can be generated without modifying the tool.

Other tools leverage MLIR for the generation of a multi-layered IR that can be optimised on different levels of abstraction and apply optimisations automatically through design space exploration (DSE). This technique relies on heuristics to explore different combinations of parameters of well known techniques, such as the unrolling factor or the size of loop tiling. ScaleHLS [18] and SODA-opt [2] are both examples of technologies which rely on this principle.

AMD Xilinx Vitis HLS is a high-level synthesis (HLS) framework that synthesises C/C++ codes into hardware. Driven by code annotations in the form of pragmas and a template library, it follows the principle of minimising the initiation interval (II), i.e. the number of cycles between iterations of a loop, to deliver performance. Vitis HLS provides a complete compilation from the LLVM C++ frontend based on Clang which generates LLVM-IR that is provided to the AMD Xilinx LLVM backend which generates HDL.

There are other non-vendor specific HLS solutions, such as Bambu HLS [10] which is also able to generate HDL from C/C++, and these follow similar principles to the Vitis HLS frontend. Fortran-HLS [15] couples the LLVM Flang frontend with AMD Xilinx’s backend to enable Fortran programming for FPGAs, with the objective of enabling HPC developers to avoid the initial time consuming step of porting their codes into C++ when targeting FPGAs. However, crucially whilst these tools tend to enable correct by construction dataflow codes, the automatic optimisation that they are able to perform is limited and so significant programmer expertise is required to obtain best performance on the FPGA.

2.2 MLIR and xDSL

Multi Level Intermediate Representation (MLIR) is an LLVM sub-project which aims to innovate in the area of Intermediate Representation (IR). For many years LLVM backends, which target specific architectures such as AMD Xilinx FPGAs, CPUs, and GPUs are connected with the language-specific frontends via LLVM-IR. However, LLVM-IR is rather low level and these language frontends, such as Clang, must undertake significant work to transform a programmer’s source code into this form. An example is leveraging FPGAs, where AMD Xilinx have had to modify the Clang front-end to provide support for their pragmas and there is very limited optimisation of the programmer’s code for a dataflow architecture.

MLIR looks to redefine the use of IRs by providing a hierarchy of IR dialects and transformations between these. First developed by Google as part of their Tensorflow project, MLIR was released open source in 2019 and became part of LLVM shortly after that. Using MLIR, frontends can generate more suitable, higher level, representations of a user’s code before this is progressively lowered through a series of dialects and ultimately LLVM-IR. Crucially, these MLIR dialects and transformations already exist and so a frontend developer needs to only generate this highest level of MLIR dialect, and can then rely on this being lowered.

MLIR provides a rich set of standard dialects, and using the framework it is possible for new dialects and transformations to be developed. Indeed, AMD Xilinx have developed their own bespoke MLIR dialect for the Versal AIE engines that integrates with their proprietary downstream compiler via lowerings. However, there is no HLS dialect that has been provided so until this work, there has been no MLIR integration with HLS for programming the PL.

However, a limitation with MLIR is that it is written in complex C++, uses an esoteric description language for definitions of dialects, and is a continually changing target due to the large development community. To this end xDSL has been developed which is a Python based compiler framework. xDSL is fully compatible with MLIR, and IRs can be moved between the two technologies seamlessly. In this paper we develop our dialects and transformations in Python using xDSL as this enables much faster prototyping of our central concepts and ideas, with these then able to be fed back into the main MLIR code-base once they are fully mature.

2.2.1 The MLIR stencil dialect. The MLIR stencil dialect enables the representation of stencil computations at the IR level. By providing this high level representation of a programmer’s mathematical problem, there is then a rich amount of information upon which the compiler has to operate.

A stencil example which sums neighbouring values in 1D is expressed with this dialect in Listing 1. This would be generated by the frontend tooling from the programmer’s description, and the stencil.load operation at line 1 loads in values into a temporary type that can be operated upon, likewise the stencil.store operation at line 11 stores resulting output back into a form that the rest of the IR can leverage. The stencil.apply operation, at line 3 defines the stencil computation itself and there are four operations that comprise the calculation. The stencil.access operations at lines 5 and 6 load a stencil value with a relative offset to the current index, here the direct neighbours, the arith.addf operation at line 7
adds these values together and this is returned for the current grid cell through the `stencil.return` operation. This `stencil.apply` operation defines the calculations that need to be undertaken on a grid cell by grid cell basis and is executed across the entire grid.

Lowerings from the PSyclone and Devito DSLs, as well as from Fortran more widely in Flang, have been developed for the stencil dialect. Furthermore, transformation passes have been developed for lowering the stencil dialect to CPUs, GPUs, and distributed memory parallelism. The programmer using these DSLs, or Flang, is able to therefore target these architectures with no additional support needed by the frontend apart from generating stencil compatible IR. It is our hypothesis that this dialect can also be used to target FPGAs, where examples such as Listing 1 contains enough contextual information such that MLIR transformations can then be written which will operate upon it and lower it to a form optimal for the dataflow architecture.

### 3 IMPLEMENTATION

In this section we explore the steps that we have developed which enable us to automatically lower stencil calculations to optimised dataflow representations on the FPGA. The overall architectural view of our approach is illustrated in Figure 1, where source code is processed by the PSyclone, Devito or Flang tools to generate the stencil dialect. Our transformation then lowers this into our HLS dialect which is lowered into annotated LLVM-IR, and then manipulated by the f++ tool, which also links against our runtime, and the resulting LLVM-IR is provided into the AMD Xilinx HLS backend. The result is an .xclbin file which contains the FPGA configuration. This comprises three main facets, our HLS dialect, the lowering from the stencil dialect to this HLS dialect, and the lowering from the stencil dialect to LLVM-IR which can then be provided to the LLVM backend.

#### 3.1 HLS dialect

Our HLS dialect replicates the high-level synthesis features provided by the AMD Xilinx Vitis tooling in a vendor agnostic way. Consequently, it is possible to lower the HLS dialect to multiple targets such as LLVM-IR (as we explore here) or CIRCT [9]. The HLS dialect currently supports the attributes sketched in Listing 2 and these describe a specific feature or facet, for instance the `hls.axi_protocol` is parameterised with the type of AXI protocol which is encoded as an i32 integer. The attribute represents the data type of a stream.

#### Listing 2: Attributes of the HLS dialect

```
<table>
<thead>
<tr>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>hls.axi_protocol</td>
<td>Protocol type for AXI interface</td>
</tr>
<tr>
<td>hls.streamtype</td>
<td>Stream data type</td>
</tr>
</tbody>
</table>
```

#### 3.1.1 Attributes

Listing 3 sketches the operations provided by our HLS dialect, and many of these will be familiar to those who acquainted with Vitis HLS. For instance, the `hls.axi_protocol` operation creates an HLS stream of type which is specified as the argument and this is returned as an `hls.streamtype` attribute. The `hls.read`, `hls.write`, `hls.empty`, and `hls.full` operations then operate upon this stream as one would expect who is familiar with Vitis HLS. The `hls.pipeline` operation can be seen, where the desired II is provided as an integer argument, as is `hls.unroll` and `hls.array_partition` which can be used to optimise for performance.

#### Listing 3: Operations of the HLS dialect

```
<table>
<thead>
<tr>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>hls.axi_protocol</td>
<td>AXI interface protocol</td>
</tr>
<tr>
<td>hls.streamtype</td>
<td>Stream data type</td>
</tr>
<tr>
<td>hls.read</td>
<td>Read operation</td>
</tr>
<tr>
<td>hls.write</td>
<td>Write operation</td>
</tr>
<tr>
<td>hls.empty</td>
<td>Empty operation</td>
</tr>
<tr>
<td>hls.full</td>
<td>Full operation</td>
</tr>
</tbody>
</table>
```

#### 3.1.2 Operations

The `hls.dataflow` operation is provided which enables the definition of dataflow regions which are then connected via streams. Whilst this MLIR dialect does not implement the full pragma set of Vitis HLS, it provides enough functionality in these ten operations such that we can leverage them to represent optimised code.

#### 3.2 Lowering the HLS dialect to LLVM-IR

In order to enable the driving of the AMD Xilinx HLS backend we had to develop a transformation which lowered from our HLS dialect to the LLVM-IR. Because existing lowerings exist for the standard MLIR dialects, such as `arith` and `math` to LLVM-IR, then aspects expressed using these, such as mathematical calculations, are already supported by the AMD Xilinx backend.

Our lowering follows the same approach adopted for connecting Flang with the AMD Xilinx backend [15], where void functions with no arguments are used to encode HLS directives. The authors of [15] chose to use functions in this manner because they then effectively become annotations in the LLVM-IR and do not alter the structure of the IR. It was found by them to be optimal compared with other approaches which did alter the IR structure and could result in a performance reduction or failure to compile. Once the LLVM-IR is generated, before providing to the AMD Xilinx HLS backend we run the f++ preprocessing tool developed in [15] to identify these corresponding function calls via pattern matching.
and replace them with the appropriate intrinsics or metadata. In some other cases it is important to take into account the structure of the IR, such as for pipelining or unrolling. These can be applied to any level of nesting in loops and, therefore, f++ makes use of LLVM passes that determine where in the loop tree the call was found to qualify the corresponding body with the necessary metadata.

An added complexity is in the handling of HLS streams, where the AMD Xilinx HLS backend only identifies a legal stream when the following two conditions hold:

1. The stream is a pointer to a structure, where the type of the stream will be the type contained within the structure, i.e. the type of the elements read and written from and to the stream will be of this type. For example, the following stream `!llvm.ptr<!llvm.struct<(f64)>>` receives and produces `f64` elements.

2. There is a call to the intrinsic `@llvm.fpga.set.stream.depth` on the first element of the stream.

To satisfy the first condition we allocate a structure to the type specified in the `hls.create_stream` operation argument. For the second requirement, we obtain a pointer to the first element of the structure with a `getelementptr` operation using offset `[0,0]`. The first index of this offset specifies the number of top-level structure type elements we are shifting in the pointer, and the second which field we pick in the structure.

3.3 HLS optimisation passes: stencil dialect to HLS dialect

The PSyclone and Devito DSLs both lower into the stencil dialect, and there has been a transformation developed for Flang that will also transform suitable loops into the stencil dialect. These transformations identify appropriate patterns and lower these into the stencil dialect. There is an existing transformation that lowers the stencil dialect into the standard MLIR dialects targeting CPU execution, and initially we added an additional step after this transformation to apply suitable constructs from the HLS dialect so that this could be handled by the AMD Xilinx HLS backend.

However, this approach was similar to those adopted by the AMD Xilinx Vitis HLS frontend and Bambu HLS, where although the code will execute correctly on the FPGA because it is still structured following the imperative Von Neumann model performance is poor. Instead, because FPGAs benefit from a dataflow approach instead [17] in which they should make progress every cycle, the IR must be organised to suit this architecture.

For stencil computations the most efficient way of organising the dataflow computation is based upon a shift buffer approach [4] [19]. Using this shift buffer, the stencil operation operates in a sliding window called a shift register instead of the data being directly accessed from external memory on demand, as in the typical CPU implementations. As such, the input field is fetched into the shift buffer until it is full, and then on every cycle required data for the current operation is provided and then a shift operation occurs where each data element is displaced one position to the right. This evicts the oldest element and a new element enters. The shift buffer has found to be an effective optimisation for these types of code, however it adds complexity for the programmer especially when working in three dimensions.

Our transformation pass that applies automatic optimisation for stencils on FPGAs operates upon the `stencil` dialect IR, like that...
shown in Listing 1, transforming into into a shift buffer pattern using the dataflow approach as illustrated in Figure 3 to ensure that the loading of data, shift buffer(s), computation, and writing of results can operate concurrently for separate elements. Our transformation involves the following steps:

(1) **Classification of kernel arguments:** Where the data arguments in a stencil region are classified as either stencil field inputs, stencil field outputs or constants.

(2) **Replacement of interface type with 512-bit packed version:** To maximise throughput in FPGAs it is important to fetch larger chunks of data, ideally of size 512-bits, each time external memory is accessed [6]. To that end, the type of the kernel interface’s argument pointers is replaced by a 512-packed version of the same type. For example, `float` double precision floating point, would be replaced by `llvm.struct<|llvm.array<8, float|>>`. This new pointer type is then propagated down through the IR to update operations that use it.

(3) **Replace direct accesses to external memory by streams:** Moving to a dataflow style of computation is a fundamental step in achieving performance, since it enables us to minimise the II in combination with the shift buffer. The transformation adds a placeholder function, `dummy_load_data`, for each stencil array that is being read and generates an HLS stream that will provide elements of data each cycle. It can be seen from Listing 23, that there are three dataflow regions running concurrently, with the first dataflow region calling out dummy function `dummy_load_data` and the second region running the shift buffer via calling the function `shift_buffer`. These operate concurrently and are connected via the `x_in` stream. The third data flow region in Listing 23, also running concurrently, extracts values from the shift buffer’s stream, `x_shift` and streams these to the compute dataflow stage. As in the illustration of Figure 3, in the cases where there are multiple compute stages operating upon the same input data then the stream is duplicated in this stage to serve each concurrently. It should be highlighted that our shift buffer does not provide a single value, but instead all the stencil values that could be required. For example, in 1 dimension three values are provided (the current grid cell and two neighbouring cells), in 2 dimensions nine values are provided, and in 3 dimensions 27 values, as shown in Figure 2.

(4) **Separation of stencil fields in the stencil.apply operation:** The stencil transformations for the CPU or GPU favour fusing stencils together for fewer, larger stencil regions. However, on the FPGA to obtain optimal throughout it is better for the calculations involved for each stencil field to be split into separate dataflow regions that can run concurrently. Therefore, we identify the result fields through the arguments of the `stencil.return` operation, and for each of the new compute loops we add a `hls.read` operation at the beginning of its body for each of the stencil input fields to read values being streamed from the shift buffer(s). Similarly, an `hls.write` operation is added to the end of the body of each loop to write the result of the resulting field to an output stream. These input and output streams are later connected to the corresponding dataflow stages.

(5) **Map stencil.access operations to the corresponding stencil value:** The `stencil.access` operation contains an offset of the form `, offset>=1, offset<=1` which determines the position of the element in the stencil with respect to the current element in the field. As the shift buffer streams all neighbouring stencil values, this transformation uses that offset to extract the required value and replace the `stencil.access` with the operations required for this.

(6) **Handle storage of results:** The `stencil.store` operations are replaced by a single call to the `write_data` dataflow function that writes data to external memory in chunks of 512-bits.

(7) **Replacement of placeholder data loading functions** Where the placeholder functions `dummy_load_data` from step item 3 are replaced by a single call to the `load_data` function which has been specialised for the number of required input fields. In order to guarantee that data loading occurs before the shift buffer operation, only the first placeholder is replaced and the remaining placeholder function calls are removed.
Hence in Figure 3 whilst there are numerous shift buffers, there is only one data loading stage.

(8) Copy small data chunks to local FPGA memory: To minimise accesses to external memory for performance, static data is copied into local FPGA BRAM or URAM if it will fit. After identifying appropriate small data chunks, it is then determined whether this is used in more than one stencil compute loop as if so it must be duplicated to provide the constraint of a single dataflow function accessing a local array. A memory reference from the memref dialect is allocated for each of these copies and this is then populated by a loop upon kernel initialisation with static elements from external memory.

(9) Assignment of input and output kernel arguments to separate bundles: To maximise bandwidth between the HLS kernel and external memory the input arguments of the kernel are looped over and the hls.interface operation is added into the IR with an AXI4 protocol. Each of these interfaces are assigned to a separate bundle to maximise bandwidth and avoid the bottleneck of a single single physical port which would result in contention as every memory access per cycle would be competing for the same port. The exception to this is for the small data which will be copied to BRAM on kernel initialisation, where this all resides in a single bundle to avoid wasting ports. Each of these ports is connected to a separate bank of HBM.

In the description of the transformation passes described in this section we have made reference to data functions such as shift_buffer, write_data and load_data. These can be found in our runtime which is linked with the generated LLVM-IR at compile time. These functions have been written in C++ and their corresponding LLVM-IR then generated which our tool then links together with the transformed programmer’s stencil code.

4 EVALUATION

The assessment of this work has been undertaken using the PSyclone DSL with two real-world 3D stencil kernels. The first is the Pi-acek and Williams (PW) advection scheme [14], commonly found in weather simulation codes, such as the Met Office’s MONC high-resolution atmospheric model [14]. Secondly we evaluate using the tracer advection scheme from the NEMO ocean model which is part of the PSyclone benchmark suite [16]. These two kernels provide different levels of complexity, for instance the PW advection scheme contains three separate stencil computations executing across three fields, whereas the tracer advection kernel comprises 24 stencil computations across six fields.

We compare our stencil-based approach against three of state-of-the-art HLS tools: DaCe, SODA, AMD Xilinx’s Vitis HLS and StencilFlow. We measure performance in million points per second (MPt/s), which is calculated as the size of the problem divided by the execution time of the kernel. The average power draw is measured in watts and calculated based upon the average of the instantaneous power draw of the card over the execution of the kernel. The energy consumed is measured in joules, and calculated as the average power draw times the execution time of the kernel.

In gathering the power and energy measurements we followed the method described in [13]. All results are averaged over 10 runs.

We run our experiments on an AMD Xilinx Alveo U280 FPGA which is being driven by the host containing a Cascade Lake Xeon Platinum 8260M CPU. We aim to maximise the use of the FPGA by replicating the compute units (CU) where possible and maintain a problem size which can fit into the U280’s 8GB of HBM. The number of CUs was limited to 4 in the case of PW advection because of the maximum number of 32 AXI4 ports supported by the Alveo U280 shell. For this benchmark each compute unit requires 7 ports, corresponding to one per field and an additional port for the small data. The exception to this mapping is with DaCe, where there is no option to replicate the number of CUs and the results that are presented are for 1 CU. The tracer advection kernel was implemented using a single CU, since each of its input arguments was mapped to a separate memory port. Whilst some ports could have been bundled together for the tracer advection benchmark to reduce the number of ports of each CU, for example reducing to 12 ports for the input and output fields plus one bundled port for the rest of the arguments would allow for 2 CUs. However this bundling would affect performance and heuristics would likely be required by our transformation to identify when to combine bundles.

Our stencil flow leverages the original PSyclone based Fortran code. Furthermore, the codes were ported to C/C++ to be compatible with SODA-opt and Vitis HLS and Python to be compatible with DaCe. All approaches used the AMD Xilinx Vitis HLS as the backend. Since Stencil-HMLS and SODA-opt generate LLVM-IR that is provided to the AMD Xilinx backend, they had to be compiled with -O0 in Vitis, as otherwise important optimisations are removed such as the copying of small data into local memory in our approach, or the II becomes large. DaCe, by comparison generates HLS C/C++ code that is used as input to the AMD Xilinx Vitis HLS frontend.

The connectivity to HBM was done manually for our approach, SODA-opt and AMD Xilinx Vitis. DaCe generates the connectivity file automatically along side the host code. However, it does not support automatic multi-bank assignment and thus the largest problem size that we measure across the technologies for the PW advection kernel can not be handled using DaCE. Supporting this would require manual construction of the SDFG, which is beyond the automatic optimisations that are part of the comparison in this section. StencilFlow presents these same limitations, as it is built atop of DaCe.

The runtime numbers for StencilFlow could not be obtained and will not be discussed in the following. Whilst PW advection could be compiled for sizes 8M and 32M they did not complete their execution under 10 minutes, a likely indicator of deadlock, and tracer advection could not be expressed in StencilFlow due to the lack of support for subselections which are a core part of this benchmark. Although it needs further development to overcome the technical challenges presented by these benchmarks, the tool is promising, reaching an II of 1 thanks to the optimisations undertaken.

Figure 4 reports the performance of the other four FPGA programming frameworks using our two benchmark kernels on the
U280 FPGA. Note that the numbers for the largest size in PW advection are missing for DaCe since it fails to compile with this framework. Stencil-HMLS delivers much higher performance than the others due to the stencil specific optimisation that were discussed in Section 3.3, where the II obtained is 1. Our approach is 90 and 100 times faster than next highest performing framework, DaCe, for the PW advection kernel when run with domain sizes of 8M and 32M respectively. Our approach is also between 14 and 21 times faster than DaCe for the tracer advection benchmark kernel for sizes 8M and 33M.

This performance difference between our approach and DaCe is partially explained by the DaCe generated code having an II of 9. Furthermore, our transformation undertakes an optimisation which splits the computation per field into separate dataflow stages which improve the overall concurrency. Thus when considering the performance difference we can express this as our approach improving by $(4(CUs) \times 9(1/9\text{ of DaCe’s II}) \times 3\text{(split)}) = 108$, which roughly approximates the advantage seen in Figure 4. The dependencies between the stencil computations in tracer advection do not allow for a clean split across components as it is applied for PW advection, which explain the reduced advantage of Stencil-HMLS over the other frameworks.

SODA-opt delivers the lowest overall performance with the PW advection benchmark, and this is because loop unrolling had to be disabled as otherwise the pipeline that was generated is too large to fit within the U280 FPGA’s resources, even when the number of full unrolls is set to 1. Moreover, the memory buffers generated by SODA-opt were disabled, as they were translated into malloc calls in the IR, which is incompatible with the AMD Xilinx HLS backend. Performance of SODA-opt and unoptimised Vitis HLS code for the tracer advection benchmark is comparable, where SODA-opt delivers the lowest overall performance with the PW advection benchmark, and this is because loop unrolling had to be disabled as otherwise the pipeline that was generated is too large to fit within the U280 FPGA’s resources, even when the number of full unrolls is set to 1. Moreover, the memory buffers generated by SODA-opt were disabled, as they were translated into malloc calls in the IR, which is incompatible with the AMD Xilinx HLS backend. Performance of SODA-opt and unoptimised Vitis HLS code for the tracer advection benchmark is comparable, where SODA-opt achieves an II of 164 and Vitis HLS of 163 on their critical path.

Figure 4: Performance comparison of the PW advection and tracer advection kernels run across the different frameworks in MPt/s (higher is better).

Figure 5: Average power draw and average energy consumption of PW advection across the different frameworks (lower is better).

Finally, it should be noted that we could expect the results for SODA-opt to be different than reflected in this experimentation if the Bambu HLS backend had been used instead of Xilinx AMD Vitis HLS. Even though the experimentation in [1] shows that the performance with of AMD Xilinx’s backend and Bambu HLS is similar, SODA-opt has progressed in the direction of a better integration with Bambu HLS ever since. We noticed that with Bambu HLS it was not necessary to remove their internal buffers, as their backend could manage malloc. Unfortunately, the shell in the U280 used for our experimentation was not supported by Bambu HLS.

5 CONCLUSIONS AND FURTHER WORK

This paper presented a multi-layered approach to automatic stencil optimisation based on MLIR. It extends the xDSL framework with the new HLS dialect that acts as a high-level abstractions for powerful concepts for FPGA performance such as task-level parallelism and pipelining. Here we present the direct lowering to LLVM IR used to synthesise the FPGA bitstream through AMD Xilinx Vitis HLS, but it opens up alternative paths for further optimisation such as lowering to CIRCT. We describe the lowering of the cornerstone of stencil optimisation in xDSL, the stencil dialect, into the HLS dialect and how this is further optimised through the FPGA-specific
Figure 6: Average power draw and average energy consumption of tracer advection across the different frameworks (lower is better).

Table 1: Resource usage for the PW advection kernel

<table>
<thead>
<tr>
<th>FRAMEWORK</th>
<th>SIZE</th>
<th>%LUTs</th>
<th>%FFs</th>
<th>%BRAM</th>
<th>%DSPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stencil-HMLS</td>
<td>8M</td>
<td>4.30</td>
<td>3.02</td>
<td>14.29</td>
<td>1.31</td>
</tr>
<tr>
<td></td>
<td>32M</td>
<td>4.31</td>
<td>3.03</td>
<td>14.48</td>
<td>1.31</td>
</tr>
<tr>
<td></td>
<td>134M</td>
<td>4.33</td>
<td>3.03</td>
<td>14.09</td>
<td>1.31</td>
</tr>
<tr>
<td>DACE</td>
<td>8M</td>
<td>8.35</td>
<td>2.00</td>
<td>5.51</td>
<td>0.49</td>
</tr>
<tr>
<td></td>
<td>32M</td>
<td>8.36</td>
<td>2.00</td>
<td>5.51</td>
<td>0.49</td>
</tr>
<tr>
<td>SODA-opt</td>
<td>8M</td>
<td>0.82</td>
<td>0.51</td>
<td>0.10</td>
<td>0.16</td>
</tr>
<tr>
<td></td>
<td>32M</td>
<td>0.82</td>
<td>0.51</td>
<td>0.10</td>
<td>0.16</td>
</tr>
<tr>
<td></td>
<td>134M</td>
<td>0.82</td>
<td>0.51</td>
<td>0.10</td>
<td>0.16</td>
</tr>
<tr>
<td>HLS</td>
<td>8M</td>
<td>1.10</td>
<td>0.52</td>
<td>0.10</td>
<td>0.12</td>
</tr>
<tr>
<td></td>
<td>32M</td>
<td>1.10</td>
<td>0.52</td>
<td>0.10</td>
<td>0.12</td>
</tr>
<tr>
<td></td>
<td>134M</td>
<td>1.11</td>
<td>0.52</td>
<td>0.10</td>
<td>0.12</td>
</tr>
<tr>
<td>StencilFlow</td>
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<td>4.80</td>
<td>3.06</td>
<td>16.87</td>
<td>3.67</td>
</tr>
<tr>
<td></td>
<td>32M</td>
<td>4.81</td>
<td>3.07</td>
<td>16.87</td>
<td>3.67</td>
</tr>
</tbody>
</table>

Table 2: Resource usage for the tracer advection kernel

<table>
<thead>
<tr>
<th>FRAMEWORK</th>
<th>SIZE</th>
<th>%LUTs</th>
<th>%FFs</th>
<th>%BRAM</th>
<th>%DSPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stencil-HMLS</td>
<td>8M</td>
<td>27.05</td>
<td>18.87</td>
<td>62.75</td>
<td>4.12</td>
</tr>
<tr>
<td></td>
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<td>27.14</td>
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</tr>
<tr>
<td>DACE</td>
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<td>11.47</td>
<td>3.65</td>
<td>10.07</td>
<td>0.68</td>
</tr>
<tr>
<td></td>
<td>33M</td>
<td>11.52</td>
<td>3.67</td>
<td>10.07</td>
<td>0.71</td>
</tr>
<tr>
<td>SODA-opt</td>
<td>8M</td>
<td>14.81</td>
<td>2.79</td>
<td>0.74</td>
<td>0.24</td>
</tr>
<tr>
<td></td>
<td>33M</td>
<td>14.77</td>
<td>2.80</td>
<td>0.74</td>
<td>0.24</td>
</tr>
<tr>
<td>HLS</td>
<td>8M</td>
<td>14.00</td>
<td>2.50</td>
<td>0.74</td>
<td>0.24</td>
</tr>
<tr>
<td></td>
<td>33M</td>
<td>14.02</td>
<td>2.50</td>
<td>0.74</td>
<td>0.24</td>
</tr>
</tbody>
</table>

transformation of shift buffers. We demonstrate through our experimentation with two real-life case studies that our approach is both performant and energy efficient compared to the state-of-the-art.

Future work includes but is not limited to:

- Explore opportunities for increased performance and/or energy efficiency gains through the lowering of the HLS dialect to CIRCT.
- Switch to a dynamic shape implementation for the stencil dialect for FPGA. The current implementation with static shape needs the generation of a new bitstream per problem size. Whilst this is not a problem with other architectures, it is time consuming with FPGAs.
- Study the performance of the optimisation when the number of memory ports is not a limiting factor. This could be tested on the AMD Xilinx VCK5000, for example, where this limitation does not exist. This would enable further replication of the kernel to better utilise the area of the device.

ACKNOWLEDGMENT

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To launch the bitstreams on the FPGA it is sufficient to compile and (other versions will work as well). HLS, depending on the tool. The host codes are written in OpenCL. 

```bash
inx Vitis HLS after the corresponding lowerings to LLVM IR or codes.
```

```
make
```

Appropriate Alveo U280 card installed.

A.1.2 Hardware dependencies. Any machine running Linux with appropriate Alveo U280 card installed.

A.1.3 Software dependencies. Python 3.10 or higher, GCC 10.2.0 (other versions will work as well).

A.1.4 Datasets. Runs were based on the PW advection and tracer advection benchmarks using the problem sizes described in this paper.

A.2 Installation

Figure 7 shows the structure of the artifact relevant for its evaluation. The four frameworks evaluated in this work, xDSL, DACE and SODA-opt are provided in their respective directories, cloned as git submodules. To install xDSL or DACE:

(1) Access xDSL or dace
(2) Run `pip install`.

The instructions to install SODA-opt are more complicated and are provided by the original authors in a README under soda-opt. All the bitstreams are ultimately synthesised using AMD Xilinx Vitis HLS after the corresponding lowerings to LLVM IR or HLS, depending on the tool. The host codes are written in OpenCL. To launch the bitstreams on the FPGA it is sufficient to compile and synthesise the host codes. Makefile are provided for all the source codes.

A.3 Experiment workflow

(1) Port the chosen kernels to the input languages of the tools: Python for DACE, C for HLS and SODA-opt and Fortran for Stencil-HMLS if we are using the PSyclone front-end.

(2) For Stencil-HMLS feed the code to xDSL and then the resulting LLVM IR to f++ to adapt it to the requirements of the AMD Xilinx Vitis HLS backend. For DACE, qualify the kernel function with the `@dace.program` decorator and apply the FPGATransformSDFG to transform the SDFG into a version amenable to FPGA. For SODA-opt run the source code through `cgeist`, from `soda-opt/polygeist` and then call SODA-opt through a script like the one provided in H2RC/benchmarks/soda-opt/pw_advection/256x256x32/run-outline-affine_for-opt_full-vitis_hls.sh. For HLS, simply compile and link with `v++`. 

(3) Compile the host OpenCL code using GCC.

(4) Execute the host code, which will launch the bitstream.

B ARTIFACT EVALUATION

The artifact of this paper can be found in https://zenodo.org/record/8272497. The structure of the directory tree of the artifact relevant for its evaluation is shown in Figure 7. The four frameworks evaluated in Section 4 are cloned in the top level as submodules in the directories dace, xdsl (Stencil-HMLS builds atop of xDSL) and soda-opt. The bitstreams used to generate the results presented in the paper are provided with the artifact, although Makefiles are also provided for their generation. They are found under the corresponding directory for each framework under `benchmarks/<framework>/<size>`, except for DACE, for which the bitstreams are found under benchmarks/dace/<size>/.dacecache/<kernel>/build. Similarly, for all the frameworks except DACE the host codes are found under benchmarks/<framework> along side a Makefile to build them. They are run with `host <size>`, where size is 0, 1 or 2 (only for PW advection), for each of the sizes presented in the paper for each problem, 0 being the smallest. For DACE the host codes are found under benchmarks/dace/<size>/.dacecache/<kernel>/ and is simply run with `host`. Alternatively, the results can be generated from scratch with the script benchmarks/run_benchmarks.py.

The plots in Section 4 can be generated from the data in benchmarks/results.json. To do so:

(2) Run `plot\_sn\_results.py`.

The bitstreams are generated differently for each framework. For Stencil-HMLS, for PW advection the all-xdsl target in the Makefile for each size lowers the code to LLVM IR through xDSL. The vitis target synthesises the LLVM IR pre-adapted by f++ and provided in the artifact. There are similar targets for tracer advection. DACE provides its own Makefiles with the target `hw` under benchmarks/dace/<size>/.dacecache/<kernel>/build. In the case of SODA-opt, we provide Makefiles with a single target that take care of the whole process. HLS also has its own Makefile.

REFERENCES

H2RC23-artifact/
  H2RC23-paper/
    plots/
      plot_sn_results.py
      util.py
    benchmarks/
      dace/
      hls/
      soda-opt/
      xdsl/
      results.json
      prepare_data_for_plotting.py
      run_benchmarks.py
      table-pw_advection-resource_utilisation.py
      table-tra_adv-resource_utilisation.py
      dace/
      soda-opt/

Figure 7: Relevant directories of the artifact for evaluation.