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Chip level characterisation studies of Ni and NiFe electrochemical deposition using test structures

J. Murray, R. Perry, J.G. Terry, S. Smith, A.R. Mount, A.J. Walton

Abstract

This paper describes the first use of test structure chips being used to characterise the fundamental properties of Ni and NiFe alloy films deposited using electroplating. This approach is used to perform a chip-level investigation into the effects of electrolyte bath composition on the characteristics of deposited Ni and NiFe layers. The advantage of this approach is that each electrolyte change does not require the replacement of a 35 litre bath (which is necessary for wafer level investigations), thereby making each experiment less time consuming and considerably cheaper to perform.

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I. INTRODUCTION

NiFe alloys are widely used in microfabricated magnetic components to increase their inductance, and are typically produced by electrochemical deposition (ECD). To help understand the electroplating of these alloys for microinductors it is first necessary to characterise the parameters controlling both Ni and NiFe deposition. This paper reports the first use of test structures electroplated on individual test chips. These have been used to characterise the plating process and evaluate parameters such as deposition efficiency, resistivity and strain in the deposited films. The key benefit of using test chips rather than full wafers is that it enables different electrolyte compositions to be evaluated in an efficient and cost effective manner.

II. TEST CHIP DESIGN AND FABRICATION

The test chip design is shown in figure 1 [1] and a 9" mask consisting of these test chips was used to pattern 8 μ m thick photoresist to form a mould for electroplating on a 200mm wafer [1]. Figure 2 shows cross sections through the structures at each stage of the process. The wafer is initially coated with a insulating layer of 0.7 μ m PECVD SiO₂, followed by a Ti:Cu:Ti seed layer stack (Ti 30 nm, Cu 200 nm). As the diced chips are to be individually plated, an additional region on chip must be exposed to accommodate the electrical contact for the potentiostat used to electroplate the chip. Therefore, two extra masks were printed on acetate, and used to expose and develop a contact pad large enough for connection to a crocodile clip. This provides electrical access to the seed layer for electroplating. It is at point the individual chips are singulated.

Before electroplating the chip, the exposed titanium layer was etched, which revealed the copper seed layer used for ECD. A schematic drawing of the diced test structure die is shown in Figure 3 where the black areas represent the exposed copper seed layer.

III. CHARACTERISATION SETUP

The electroplating/measurement system used consisted of a computer controlled potentiostat/ galvanostat (Metrohm Autolab PGSTAT302), pH meter (Mettler Toledo), digital thermometer and a three electrode system with a saturated calomel electrode (SCE) as reference electrode (RE), a pure nickel pellet with surface area of 3 cm² as the counter electrode (CE - anode) and a test structure chip as the working electrode (WE - cathode). The nickel anode was used instead of inert platinum in order to be consistent with plating procedures used for wafer-scale processes. This setup was kept identical for all experiments with the spacing between the CE and WE set at 2.5 cm. The cell used was a 200 ml, temperature controlled beaker with 100 ml of electrolyte. The solution was purged to

remove dissolved air by bubbling argon gas for about 20 minutes. For most tests the current density applied ranged between 5 and 40 mA/cm², the temperature was 25 °C and the pH of the electrolyte was between 2.4 and 2.6. As the pH tends to increase after ECD due to hydrogen evolution at the cathode surface it was kept constant by adding measures from a 1% HCl solution.

The electrolyte combinations evaluated are detailed in table 1. A fresh bath was used for each batch of chips and the plated samples were rinsed with deionised water and dried using a flow of nitrogen gas, after which they were taken for further characterisation.

The plating current efficiency was first established from the mass gain of the cathode (the test chip in figure 3) by comparing the weight of the chip before and after the ECD process. After this the photoresist was stripped, the seed layers were etched and the strain test structures were released by HF vapour etching of the sacrificial SiO₂ layer as detailed in reference [1]. Figure 4 shows a SEM of some released test structures.

The pointer arm rotation of the strain test structures was determined from a photographic picture of the structure using an image analysis algorithm written in Labview, which is described in reference [2]. To ensure that arm geometry did not affect the results, a single device geometry was analysed (separation ratio $\Delta Y/W = 1.75$).

In addition magnetic hysteresis of the plated film was also determined using a B-H loop measurement system.

IV. EFFECTS OF PLATING CONDITIONS AND ADDITIVES

A limited number of ECD tests were performed at room temperature, to investigate the effect of changing nickel(II) concentrations on plating efficiency and the resulting film strain. The bath setup was kept free of any additives or surfactants. Three sets of test structure chips were plated, all with the same target thickness (5 μ m) but with varying plating current densities (5, 7, 10, 20, 40 mA/cm²). Each set represents a different bath concentration of NiCl₂ (0.1M, 0.4M and 1.0M). Chips from each set were plated galvanostatically at the set current densities, for the time calculated at 100% plating efficiency to achieve a target thickness of 5 μ m.

The test chips enabled the extraction of parameters such as plating efficiency, shown in Figure 5 for the different baths. Another example of the measurements made is the pointer arm rotation (strain) measurements where each chip evaluated had the seed layer stripped and the test structures released. Microscope images were used to extract the pointer arm rotation (strain).

The general trend of strain, from the pointer arm rotation with respect to plating current density for the three baths can be seen from the plot in Figure 6.

V. CONCLUSIONS AND FURTHER WORK

This abstract has detailed the first reported use of individually plated test chips being employed to characterise electroplating technology. The full paper will include existing result of the comparison of measurement on test chips using the electrolyte recipes in section III.

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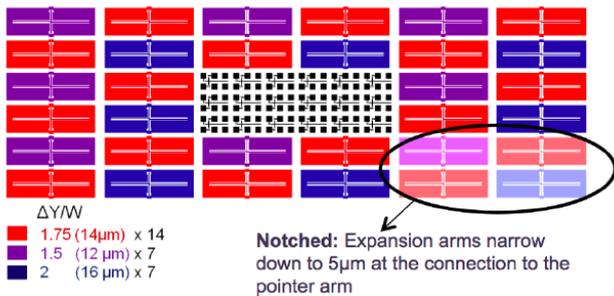


Figure 1. Chip layout with 32 pointer arm strain sensors of three different $\Delta Y/W$ ratios (colour coded) surrounding 6×3 electrical test structures in the middle

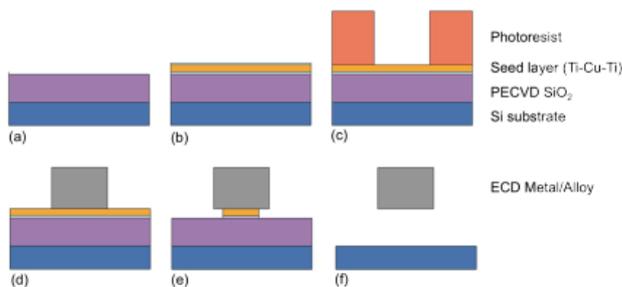


Figure 2. Schematic process flow showing cross sections through a test structure at each stage of fabrication (a) PECVD oxide deposition (b) seed layer (c) resist patterning (d) electrodeposition (e) seed layer wet etch (f) test structure release using HF vapour etch.

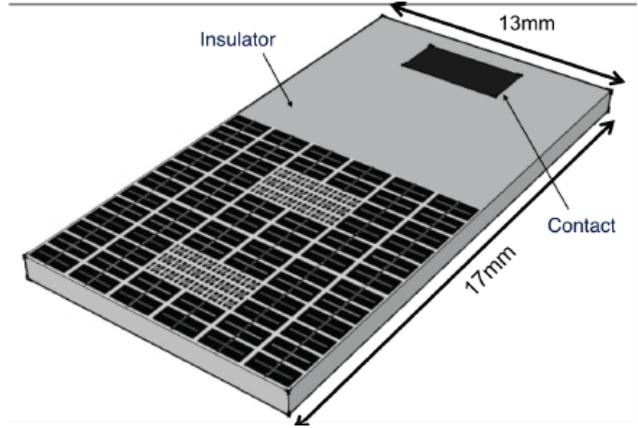


Figure 3. Schematic drawing of a diced test structure die with 64 strain sensors and 36 electrical test structures giving a total surface area of 0.765cm^2

TABLE I: ELECTROPLATING BATH COMPOSITIONS

Experiment	Bath Composition
1	NiCl_2
2	NiCl_2 -boric acid
3	NiCl_2 -saccharin,
4	NiCl_2 -boric acid-saccharin,
5	NiCl_2 - FeCl_2 ,
6	NiCl_2 - FeCl_2 -boric acid,
7	NiCl_2 - FeCl_2 -saccharin
8	NiCl_2 - FeCl_2 -boric acid-saccharin

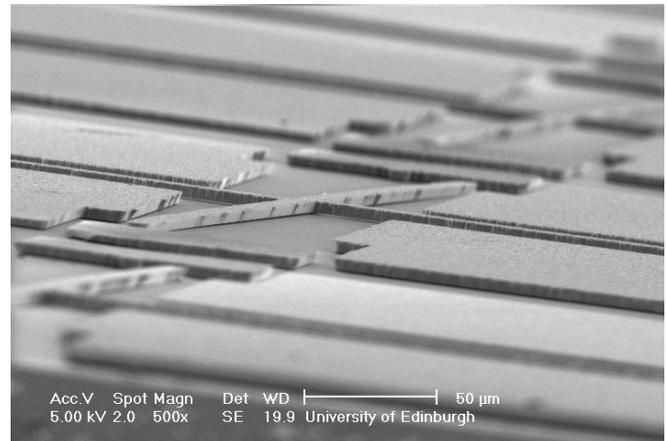


Figure 4. ECD NiFe ($5\mu\text{m}$ thick) SEM image of top showing the rotation of pointer arm after HF vapour release

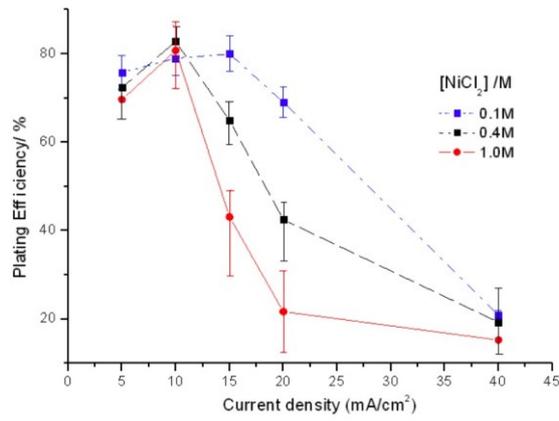


Figure 5. Efficiency of nickel baths with composed of different NiCl_2 compositions 0.1M, 0.4M and 1.0M at pH of 2.6

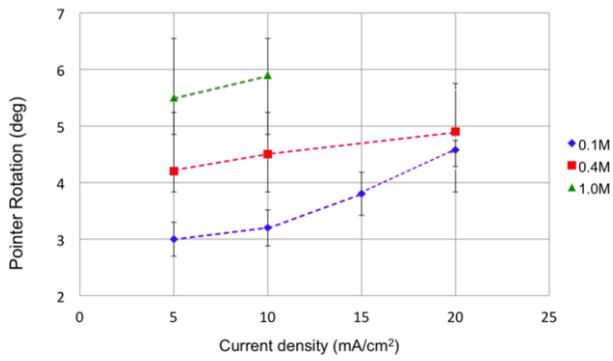


Figure 6. Pointer rotation of nickel test structures plated in different nickel(II)chloride compositions 0.1M, 0.4M and 1.0M at pH of 2.6