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Towards the Synthesis of Coherence/Replication Protocols from Consistency Models via Real-Time Orderings

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Abstract
This work focuses on shared memory systems with a read-write interface (e.g., distributed datastores or multiprocessors). At the heart of such systems resides a protocol responsible for enforcing their consistency guarantees. Designing a protocol that correctly and efficiently enforces consistency is a very challenging task. Our overarching vision is to automate this task. In this work we take a step towards this vision by establishing the theoretical foundation necessary to automatically infer a protocol from a consistency specification. Specifically, we propose a set of mathematical abstractions, called real-time orderings (rt-orderings), that model the protocol. We then create a mapping from consistency guarantees to the minimal rt-orderings that enforce the guarantees. Finally, we informally relate the rt-orderings to protocol implementation techniques. Consequently, rt-orderings serve as an intermediate abstraction between consistency and protocol design, that enables the automatic translation of consistency guarantees into protocol implementations.

CCS Concepts → Computer systems organization → Cloud computing; Multicore architectures; Software and its engineering → Consistency.

Keywords: Consistency; Coherence; Replication; Synthesis;

1 Introduction
This work focuses on “shared memory” systems that provide a read/write interface to the programmer. Such systems are ubiquitous in both computer architecture and distributed systems. Prominent examples include shared memory multiprocessors (SMPs), GPUs, NoSQL Databases [1], coordination services[9], and software-based DSMs [10].

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Figure 1: a) The producer-consumer synchronization pattern mandates that if P2 reads P1’s write to \( y \), then it must also read P1’s write to \( x \). b) The independent-reads independent-writes (IRIW) pattern mandates that if P2 sees P1’s writes but not P3’s and P4 sees P3’s write, then P4 must see P1’s write.

Such systems commonly replicate data—sometimes for performance (through caching), sometimes for fault tolerance and sometimes for both. To enable reasoning in the presence of replication, a memory consistency model (MCM) is specified as part of the system’s interface, providing the rules that dictate what values a read can return. In order to enforce the MCM, the system deploys a protocol which ensures that the replicas behave in accordance to the MCM. This protocol is called coherence protocol in computer architecture and replication protocol in distributed systems. We simply refer to it as the protocol.

The MCM specifies the behaviour of the system when executing parallel programs by enumerating all patterns through which parallel programs can synchronize. For example, an MCM \( CM_a \) can guarantee the synchronization pattern of Figure 1a (commonly known as “producer-consumer”). Specifically, in Figure 1a, process P1 writes object \( x \) and then \( y \), while process P2 reads \( y \) and then \( x \). \( CM_a \) guarantees that if P2’s read to \( y \) returns the write of P1, then P2’s read to \( x \) will also return the write of P1 (i.e., \( x = 1 \)).

The MCM is thus a contract between the programmers and the designers. While programmers must understand the behaviour of the system, the designers must understand how to implement that behaviour. Problematically, enforcing the MCM is very challenging. For instance, consider two well known MCMs: TSO [18] and Causal Consistency (CC) [19]. TSO enforces both Figure 1a and b while CC enforces Figure 1a but not b. Given this information, how is the designer to implement a correct and efficient protocol for either MCM? Crucially, how is the designer to differentiate between the two models? E.g., how can one exploit that Figure 1b need not be enforced in the CC protocol?
Our overarching vision is to automate the above task: given a target MCM we envision a software tool that can produce an efficient protocol. We argue that to create this tool we need one additional level of abstraction which can act as an intermediary between the MCM and the protocol. That is: (1) we must be able to automatically translate any MCM to this abstraction; and (2) we must also be able to map the abstraction itself into protocol design choices. In this work, we take a step towards actualizing our vision, by proposing such an abstraction and, most crucially, presenting the mapping from MCMs to this abstraction. We also informally relate the abstraction to protocol design choices.

To create this abstraction, we observe that a shared memory system, be it a multiprocessor or a geo-replicated Key-Value Store (KVS), can be abstracted through the model of Figure 2, which depicts a set of processes executing a parallel program. Each process inserts its memory operations to a structure we call the reorder buffer (ROB), allocating one ROB entry per operation. The memory system executes the operations it finds in the ROB and writes back the response of each operation in-place in its dedicated entry.

A process models a client of a KVS or a core of a multiprocessor. The ROB abstracts the core’s load-store queue or a software queue that a KVS must maintain to keep track of incoming requests. The memory system is modelled as a distributed system comprising a set of nodes, where each node contains a controller and a memory. The nodes model the private caches of the multiprocessor or the geo-replicated memory servers of the KVS. Finally the network of the memory system can be thought of as the Network-on-Chip or as the WAN.

We observe that protocols of real systems enforce various consistency models using two widgets: 1) the ROB that allows for the reordering of operations; and 2) the memory system which determines how a read or a write executes, i.e., how it propagates to each of the replicas. We propose two sets of mathematical rules to abstract protocols, one that can abstract the reorderings of the ROB and one that can abstract the propagation rules of the memory system.

Specifically, we model the ROB using four rules named program-order real-time orderings (prt-orderings). The prt<sub>WR</sub>, prt<sub>RR</sub>, prt<sub>W</sub>, and srt<sub>W</sub> mandates that when write w precedes read r in a program execution, then r can begin executing in the memory system only after w has completed. Similarly, we define srt<sub>WR</sub>, srt<sub>RR</sub>, srt<sub>W</sub>, for the rest of the combinations between reads and writes. To summarize, we model an ROB by specifying the subset of the four prt-orderings it enforces.

We model the memory system using four rules named synchronization real-time orderings (srt-orderings). The srt<sub>WR</sub>, srt<sub>RR</sub>, srt<sub>W</sub>, and srt<sub>W</sub> mandates that if write w to object x completes before read r to object x in real time, then r must observe w. Similarly, we define srt<sub>WR</sub>, srt<sub>RR</sub>, srt<sub>W</sub>. To summarize we model a memory system by specifying the subset of the four srt-orderings it enforces.

We refer to prt-orderings and srt-orderings as real-time orderings (rt-orderings). The eight rt-orderings comprise our designer-centric intermediate abstraction of the protocol.

While the rt-orderings have been employed by other works in the past to model consistency models or protocols (§9), this work is the first to present a mapping from MCMs to the rt-orderings. That is, given any MCM, we provide the set of minimal rt-orderings that enforce it. Crucially, this mapping, along with relating the rt-orderings with protocol implementation techniques, pave the way for automating protocol design.

Using this mapping from MCMs to rt-orderings, we now revisit the questions we posed on Figure 1. Specifically, prt-orderings prt<sub>WR</sub>, and srt-ordering srt<sub>W</sub> suffice to enforce the producer-consumer pattern (discussed in Section 5.4). Informally, prt<sub>WR</sub>, mandates that writes from the same process must be executed in the order intended by the program; prt<sub>RR</sub>, mandates the same for reads; srt<sub>W</sub> mandates that a read must be able to return the value of the latest completed write (from any process). To also enforce the IRIW pattern, srt<sub>R</sub>, is required (discussed in Section 5.5). Informally, srt<sub>R</sub>, mandates that if a read returns the value of write w, then any later read must also be able to return the value of write w.

Contributions. In summary, in this work we make the following contributions:

- We propose and formalize eight rt-orderings for mathematically modelling consistency enforcement protocols, serving as an intermediate abstraction between the MCM and the protocol implementation (§3).
- We create a mapping from MCMs to rt-orderings, specifying the minimal set of rt-orderings sufficient to enforce any MCM (§5) and vice versa, specifying the MCM enforced by any set of rt-orderings (§6).
- We informally map rt-orderings to protocol implementation techniques (§7).
2 Preliminaries

In this section, we first establish the system model, then we describe the notation we will use throughout the paper and finally we discuss how executions are modeled.

2.1 System Model

Figure 2 illustrates our system model. Specifically, there is a set of $P$ processes, each of which executes a program and there is a protocol which enforces the MCM. The protocol is comprised of a set of reorder buffers (ROBs) and the memory system. The memory system stores a set $X$ of shared objects, each of a unique name and value. A memory operation (or simply operation) can be either a read or a write of an object. A read returns a value and a write overwrites the value of the object and returns an ack.

ROBs. The ROBs are used to facilitate communication between the processes and the protocol. There are three events in the lifetime of an operation within the ROB: issuing, begin and completion. Specifically, we write that a process "issues an operation", when the operation is first inserted in the ROB. A process pushes operations in the ROB in the order that they are encountered within its program. We refer to this order as the program order. Furthermore, we write that "an operation begins" when the memory system begins executing the operation. In this case the memory system marks the operation’s ROB entry as beginned. Similarly, we write that "an operation completes" when the memory system has finished executing the operation. In this case, the memory system marks the operation’s ROB entry as completed (and writes back the result if it is a read).

Notably, a process can use the value returned by a read, as soon as the read is marked completed by the memory system, irrespective of whether preceding operations are completed. An operation is removed from the ROB, if all three conditions hold: 1) it is the oldest operation, 2) it is completed and 3) the process has consumed its value, if it is a read.

Memory system. We model the memory system as a distributed system comprised of a set of nodes, where each node contains a controller and a memory. Furthermore, each node is connected to one ROB, from which it reads the operations that must be executed. The controller of each node is responsible for the execution of the operations. The memory of each node stores every object in $X$.

2.2 Notation

The notation used throughout this paper is the one used by Alglave et al. [2]. We repeat it here for completeness. The notation is based on relations. Specifically, we will denote the transitive closure of $r$ with $r^*$ and the composition of $r_1$, $r_2$ with $r_1; r_2$. We say that $r$ is acyclic if its transitive closure is irreflexive and we denote by writing $acyclic(r)$. Finally, we say that $r$ is a partial order, when $r$ is transitive and irreflexive.

We say that a partial order $r$ is a total order over a set $S$, if for every $x, y$ in $S$, it is that $(x, y) \in r \lor (y, x) \in r$.

We use small letters to refer to memory operations (e.g., $a$, $b$, $c$ etc.). In figures that show executions (e.g., Figure 3), we denote a write with $W_x = val$ where $x$ is the object to be written and $val$ is the new value. Similarly, reads are represented as $R_x = val$, where $val$ is the value returned. When required relations between operations are denoted with red arrows in figures.

2.3 Modelling executions

To model executions, we use the framework created by Alglave et al. [2], introducing minor changes where necessary. Specifically, we model an execution as a tuple($M$, $po$, $rf$, $hb$, $RL$). $M$ is the set of memory operations included in the execution, $po$, $rf$ and $hb$ are relations over the operations and $RL$ is a set of relations $rl$ over the operations.

Execution relations ($po$, $rf$, $hb$ and $rl$). The program order $po$ relation is a total order over the operations issued by a single process, specifying the order in which memory operations are ordered in the program executed by the process. Operations are issued by a process in this order. Only operations from the same process are ordered. For two operations $a, b$ from process $i \in P$, if $a$ is issued before $b$ then $(a, b) \in po$.

The reads-from $rf$ relation contains a pair for each read operation in $M$, relating it with a write on the same object. For the pair $(a, b) \in rf$, it must be that $a$ is a read that returns the value created by the write $b$, i.e., a reads-from $b$.

The happens-before $hb$ relation is a partial order over all operations, specifying the real-time relation of operations. Specifically, for two operations $a, b$, if $(a, b) \in hb$, then that means that $a$ completes before $b$ begins.

Finally, the read-legal $rl$ relation is a total order over all operations, with the restriction that acyclic($rl \cup rf$). Given the $rf$ of an execution $E$, it is often possible to construct more than one $rl$. We associate each execution $E$, with a set $RL$ which contains every $rl$ that can be constructed from $E$. For each $rl \in RL$, we derive the following relations.

Relations derived from $rl$ ($ws$, $fr$, $syn$). The write-serialization $ws$ relation is a total order of writes to the same object that can be derived from $rl$, such that $ws \subseteq rl$. Intuitively, $ws$ captures the order in which writes to the same object serialize.

The from-reads $fr$ relation connects a read to writes from the same object that precede the read in $rl$. Specifically, for every read $a$ and a write $b$ to the same object where $(a, b) \in rl$, then $(a, b) \in fr$. It follows that $fr$ is transitive and $fr \subseteq rl$.

Finally, the synchronization $syn$ relation combines the $rf$, $fr$ and $ws$ relations. Specifically, $syn$ is a partial order over operations on the same object defined as the transitive closure of the union of $rf$, $ws$ and $fr$, i.e., $syn \triangleq (rf \cup ws \cup fr)^*$. Two operations on the same object are said to synchronize if
one of them is a write. Formally, for any pair of operations \((a, b)\) on the same object, if at least one of \(a, b\) is a write then it must be that \((a, b) \in \text{syn} \lor (b, a) \in \text{syn}\). If both \(a, b\) are reads, then \((a, b) \in \text{syn}\) iff there exists a write \(c\), such that \((c, a) \in \text{syn} \land (c, b) \in \text{syn}\).

**Helper relations (po-type, syn-type, hb-type).** Given the set of operations \(M\), we define four relations \(WW, WR, RR, RW\) over \(M\) that contain all write-write, write-read, read-read and read-write pairs found in \(M\), respectively. Table 2 uses these four relations to define the po-type, syn-type and hb-type relations. Specifically, by taking the intersection of po with each of \(WW, WR, RR, RW\), we define \(po_{ww}, po_{wr}, po_{rr}, po_{rw}\). We write po-type as a placeholder that can be replaced by any of these four relations. Notably, every pair in po is also in one of the po-type relations. I.e.,

\[
\text{po} \triangleq \text{po}_{ww} \cup \text{po}_{wr} \cup \text{po}_{rr} \cup \text{po}_{rw}
\]

Similarly, we define syn\(_{wr}\) and syn\(_{rr}\). Note that we do not need to define syn\(_{ww}\) and syn\(_{rw}\), because they would be the same as \(ws\) and \(fr\), respectively. We write syn-type as a placeholder for \(ws, \text{syn}_{wr}, \text{syn}_{rr}, fr\). We note that every pair in syn is also in one of the syn-type relations and that \(fr\) is a subset of syn\(_{wr}\).

\[
\text{syn} \triangleq \text{ws} \cup \text{syn}_{wr} \cup \text{syn}_{rr} \cup \text{fr} \\
fr \subseteq \text{syn}_{wr}
\]

Finally, in the same spirit, we define the hb-type relations:

\[
\text{hb}_{ww}, \text{hb}_{wr}, \text{hb}_{rr}, \text{hb}_{rw}.
\]

### 3 Real-time orderings

In this section we introduce and formally define the real-time orderings (rt-orderings), through which we model the protocol. There are two types of rt-orderings: the program-order real-time orderings (prt-orderings) through which we model the operation of the ROB and the synchronization real-time orderings (srt-orderings), through which we model the operation of the memory system. Table 1 provides the definition of each of the eight rt-orderings. Below we first describe the prt-orderings and then the srt-orderings.

#### 3.1 Program-order Real-time Orderings

An execution \(E(M, po, rf, hb, RL)\) is said to enforce the prt\(_{wr}\) if:

\[
\forall w, r \in M \text{ s.t. } (w, r) \in \text{po}_{wr} \rightarrow (w, r) \in \text{hb}_{wr}
\]

Plainly, a read \(r\) cannot begin before all writes that precede it in program order have completed. Table 1 extends this definition to write-write, read-read and read-write pairs. When all four prt-orderings are enforced then it follows that \(po \subseteq hb\).

#### 3.2 Synchronization Real-time Orderings

The synchronization real-time orderings (srt-orderings) are constraints over operations to the same object. There are four srt-orderings: \(srt_{ww}, srt_{wr}, srt_{rr}, srt_{rw}\). An execution \(E(M, po, rf, hb, RL)\) enforces the srt-ordering \(srt_{wr}\) if there exists \(rl \in RL\) such that:

\[
\text{acyclic}(\text{hb}_{wr} \cup \text{syn})
\]

In other words the \(srt_{wr}\) mandates that for a write \(a\) and a read \(b\) if \((a, b) \in \text{hb}_{wr}\), then it must be that \((b, a) \notin \text{syn}\). Table 1 describes the condition required to enforce each of the srt-orderings. A memory system is said to enforce an srt-ordering, if that srt-ordering is enforced in every execution that can be generated by the memory system. Notably, a combination of the srt-orderings can be enforced, for example \(srt_{ww}, srt_{rw}\) are both enforced when \(\text{acyclic}(\text{syn} \cup \text{hb}_{ww} \cup \text{hb}_{wr})\). When all four srt-orderings are enforced then linearizability is enforced \([8]\) (we expand on this on Section 8.1).

### 4 Memory consistency models (MCMs)

In order to create a mapping from memory consistency models (MCMs) to the rt-orderings we need to establish a formalism for the MCMs. In this section, we use the formalism of Alglave et al. \([2]\) to describe *synchronization patterns* (sync-pats) and assert that any MCM \(CM\) is defined as a set of sync-pats \(S_{CM}\). An execution enforces \(CM\) iff it enforces every sync-pat in \(S_{CM}\). Below we define what a sync-pat is and what its enforcement entails.

A sync-pat is a path between two operations to the same object. The path can be constructed through any composition of po-type and syn-type relations, with the only restriction being that at least one po-type must be included (explained in the remarks below). Table 2 describes which relations are denoted po-type and syn-type.

For example, consider the sync-pat \(s\) that consists of a \(po_{wr}\) relation, then an \(fr\) relation and then a \(po_{rw}\) (depicted in Figure 3a). We can describe \(s\) by composing the three relations as follows:

\[
s \triangleq po_{wr}; fr; po_{wr}
\]
Initially $x = 0, y = 0$

Given an execution $E(M, po, rf, hb, RL)$, we assert that $E$ enforces $s$ if there exists $rl \in RL$ from which we can derive a syn such that:

acyclic($s \cup syn$)

In other words, a sync-pat that starts from operation $a$ and ends on operation $b$ is said to be enforced if $(b, a) \notin syn$.

Figure 3 depicts four sync-pats to serve as examples. In the execution of Figure 3a, the sync-pat occurs between operations $a$ and $d$. In this instance, $s$ is enforced because $d$ returns the value created by $a$. If $d$ were to return 0, that would mean that there is a syn relation between $d$ and $a$ and thus $s$ is not enforced.

Remarks. Note the following two remarks. First, we use syn rather than rl to test whether a sync-pat is enforced. This is because the sync-pat is a path between two operations to the same object, but rl is a total order of all operations across all objects. Second, note that a sync-pat must have at least one po-type, because otherwise it would just be a composition of syn-type relations. Any such composition is a subset of syn, which means that the execution enforces it by definition.

Consistency models. An MCM $CM_i$ is defined by asserting that a set of sync-pats $S_{CM}$ must be enforced. Plainly, an execution enforces $CM_i$ if it enforces every $s \in S_{CM}$. As an example, assume that $CM_i$ is defined through the four sync-pats depicted in Figure 3, which are formalized as follows:

$s_1 \triangleq po_{wr}; fr; po_{wr}$, $s_2 \triangleq po_{wr}; rf; po_{rw}$,

$s_3 \triangleq po_{rw}; ws; po_{wr}$, $s_4 \triangleq po_{rr}; syn_{rr}; po_{rw}$

We define $CM_i$ to be the following rule:

acyclic($s_1 \cup syn$) $\land$ acyclic($s_2 \cup syn$)

$\land$ acyclic($s_3 \cup syn$) $\land$ acyclic($s_4 \cup syn$)

5 From MCMs to rt-orderings

In this section, we provide a mapping from MCMs to rt-orderings. Specifically, given an MCM $CM_i$ that is specified through a set $S_{CM}$ of sync-pats, we automatically infer a set of rt-orderings, sufficient to enforce $CM_i$. In the rest of this section, we first differentiate between regular and irregular sync-pats (§5.1). Then we provide the mapping (§5.2), prove its correctness for an example sync-pat (§5.3), extend the proof to all regular sync-pats (§5.4) and finally extend the proof to irregular sync-pats (§5.5). In Table 3, we provide the mapping of 16 sync-pats to rt-orderings.

5.1 Regular and irregular sync-pats

We first categorize sync-pats into two classes: regular and irregular. A regular sync-pat is 1) composed by alternating po-type and syn-type relations and 2) starts and ends on a po-type. Thus, any regular sync-pat $s$, is of the following form:

$s \triangleq$ po-type; syn-type; po-type; ... syn-type; po-type

Any sync-pat that does not conform to regularity rules is irregular. The distinction between regular and irregular sync-pats will aid in the presentation of the mapping from sync-pats to rt-orderings. Specifically, we will first create a mapping from a regular sync-pat to the sufficient rt-orderings to enforce it. Then, in order to use the same mapping for irregular sync-pats, we will show that for every irregular sync-pat $s_i$, there exists a regular sync-pat $s_r$, such that enforcing $s_r$ is sufficient to enforce $s_i$.

5.2 The mapping

We assert the following three conditions to enforce any regular sync-pat, assuming that an operation can be of type $m$ or $n$ where $m, n \in \{read, write\}$.

- **Cond-1:** For every po-type relation $po_{mn}$ found in $s$, the corresponding prt-ordering $prt_{mn}$ must be enforced. Plainly any po-type relation must also be an $hb$ relation.
- **Cond-2:** For every syn-type relation $syn_{mn}$, if it is not an $rf$, the reverse srt-ordering $srt_{nm}$ must be enforced.
- **Cond-3:** If the first operation in $s$ is of type $m$ and the last of type $n$, the corresponding srt-ordering $srt_{nm}$ must be enforced.

5.3 Proof for an example sync-pat

We will start by first proving that the three conditions are sufficient for the simple sync-pat, that is portrayed in Figure 3a. Then we will extend to any regular sync-pat. The simple sync-pat $s$ is the following:

$s \triangleq po_{wr}; fr; po_{wr}$

For $s$ the three conditions require the following rt-orderings:

- **Cond-1:** The $prt_{wr}$ is required for both $po_{wr}$ relations.
- **Cond-2:** The $srt_{wr}$ for the $fr$ (i.e., $syn_{wr}$) relation.
- **Cond-3:** The $srt_{wr}$ because $s$ starts with a write and ends on a read.
We sketch a proof for this rule using Figure 4a. Figure 4a shows a timestamp $(\text{ht}, \text{bb})$ which is associated with a timestamp $(\text{ta},\text{tb},\text{tc},\text{td})$. Let's assume that $(\text{ta} < \text{tb})$ and $(\text{tb} < \text{tc})$. Operation $b$ begins before $c$ completes and $d$ begins before $b$ completes. Therefore it suffices to prove that cond-1 and cond-2 guarantee the above condition. We will do so by proving that $(a, b) \in (\text{ht}, \text{bb})$.

Firstly, cond-1 $(\text{prt}_w)$ mandates that $\text{po}_w \subseteq \text{hb}_w$. Therefore, $(a, b), (c, d) \in \text{hb}$. We need only prove that $(b, c) \in \text{bbc}$. Let’s assume that $(b, c) \notin \text{bbc}$. It follows that $(c, b) \in \text{hb}$. Recall, that $b$ is a write and $c$ is a read. Cond-2 mandates that $\text{srt}_w$ is enforced: since $(c, b) \in \text{hb}$ then $(b, c) \notin \text{syn}$. We have reached a contradiction, and therefore it must be that $(b, c) \in \text{bbc}$.

Figure 4b provides the counter-example where $(b, c) \notin \text{bbc}$. In this case it cannot be that $(a, d) \in \text{s}$ because $(b, c) \in \text{hb}$ and therefore from cond-2 it follows that $(c, b) \in \text{syn}$. Plainly, the sync-pat $\text{s}$ will not occur here because P1’s read to $y$ will observe P2’s write to $y$.

As we have shown above, from cond-1 and cond-2 it follows that $(a, d) \in \text{hb}$ and thus from cond-3 it follows that $(a, d) \notin \text{syn}$. Therefore the three conditions are sufficient to enforce $\text{s}$.

5.4 Extending to all regular sync-pats
Note the intuition behind the three conditions. Cond-1 ensures that every $\text{po}$-relation of the sync-pat is also an $\text{hb}$ relation. Similarly, cond-2 ensures that every $\text{syn}$-relation is also a $\text{bbc}$ relation. As a regular sync-pat is composed by alternating $\text{po}$- and $\text{syn}$-relations, enforcing cond-1 and cond-2 ensures that the sync-pat can be expressed as a composition of alternating $\text{hb}$ and $\text{bbc}$ relations.

As we saw $\text{hb}$; $\text{bbc}$; $\text{hb}$; $\text{hb}$ by induction we can extend this rule for any sequence of alternating $\text{hb}$ and $\text{bbc}$ relations. Specifically:

\[
\forall a, b \in M \text{ s.t. } (a, b) \in (\text{hb}; \text{bbc}; \text{hb}) \rightarrow (a, b) \in \text{hb}
\]

Therefore, cond-1 and cond-2 ensure that if $(a, b) \in \text{s}$ then $(a, d) \in \text{hb}$ for any regular sync-pat $\text{s}$. Finally, cond-3 ensures that the sync-pat is enforced, by ensuring that if $(a, d) \in \text{hb}$ then $(b, a) \notin \text{syn}$.

5.5 Extending to irregular sync-pats
A sync-pat is deemed irregular if 1) it has consecutive $\text{po}$-relations or 2) it has consecutive $\text{syn}$-relations or 3) it does not start with a $\text{po}$-relation (i.e., starts with
syn-pat} with the same relations. Therefore, for any sync-pat \( \{a, b, c\} \) and the second \( \text{po-type} \) includes \( (c, d) \). The highlighted cell corresponds to Figure 3a.

<table>
<thead>
<tr>
<th>( c \rightarrow Wx )</th>
<th>( c \rightarrow Wx )</th>
<th>( c \rightarrow Ry )</th>
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<td>( b \rightarrow Rx )</td>
<td>( pr_{tw} )</td>
<td>( pr_{tw} )</td>
<td>( pr_{tw} )</td>
</tr>
<tr>
<td>( a \rightarrow Wx )</td>
<td>( st_{rw} ), ( st_{tw} )</td>
<td>( st_{tw} )</td>
<td>( st_{tw} )</td>
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<tr>
<td>( b \rightarrow Rx )</td>
<td>( pr_{tw} ), ( pr_{tw} )</td>
<td>( pr_{tw} ), ( pr_{tw} )</td>
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<tr>
<td>( a \rightarrow Rx )</td>
<td>( st_{tw} ), ( st_{tw} )</td>
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<tr>
<td>( b \rightarrow Wx )</td>
<td>( pr_{tw} ), ( pr_{tw} )</td>
<td>( pr_{tw} ), ( pr_{tw} )</td>
<td>( pr_{tw} )</td>
</tr>
</tbody>
</table>

Table 3: The mapping of 16 sync-pats to rt-orderings. Each cell represents a sync-pat of the form \( s \) \( \triangleq \) \text{po-type}; \text{syn-type}; \text{po-type}, where the first \text{po-type} includes \( (a, b) \), the \text{syn-type} includes \( (b, c) \) and the second \text{po-type} includes \( (c, d) \).

**Consecutive \text{po-type}.** We start with sync-pats with consecutive \text{po-type} relations. We use the insight that any composition of \text{po-type} relations must be the subset of one of \( po_{wr}, po_{rw}, po_{rr} \) relation. For instance \( po_{wr} ; po_{rw} ; po_{rr} \) is a subset of \( po_{wr} \). Therefore, for any \( s \) that has consecutive composed \text{po-type} relations, we derive a \( \text{po-type} \) which replaces them with a single \text{po-type} relation, such that \( s \subseteq s' \) and we assert that enforcing \( s' \) is sufficient to also enforce \( s \). Below is an example of \( s \) and the derived \( s' \) using the insight that \( (po_{wr};po_{rw}) \subseteq po_{wr} \).

\[
\begin{align*}
s & \triangleq po_{wr}; po_{rw}; syn_{wr}; po_{rr} \\
s' & \triangleq po_{wr}; syn_{wr}; po_{rr}
\end{align*}
\]

Note that an alternative approach would have been to omit deriving \( s' \) and instead simply asserting that the first condition is applied for each \text{po-type} relation in \( s \). That would still be correct and can be used.

**Consecutive \text{syn-type}.** Our approach is identical for sync-pats with consecutive composed \text{syn-type} relations. Specifically, a composition of \text{syn-type} relations is always a subset of one of \( fr, ws, syn_{wr}, syn_{rw} \). This is because any pair in a composition of \text{syn-type} relations is also in \text{syn} and thus it must be in one of \( fr, ws, syn_{wr}, syn_{rw} \), as \text{syn} is the union of these four relations. Therefore, for any \( s \) that has consecutive composed \text{syn-type} relations, we derive an \( s' \) which replaces them with a single \text{syn-type} relation, such that \( s \subseteq s' \).

**Begin with \text{syn-type}.** When a sync-pat \( s \) begins with a \text{syn-type} relation, then we derive \( s' \) by simply removing it. Let us see why through an example. Assume the following \( s \) which starts with an \( fr \) and the derived \( s' \) which removes the \( fr \):

\[
\begin{align*}
s & \triangleq fr; po_{wr}; fr; po_{wr} \\
s' & \triangleq po_{wr}; fr; po_{wr}
\end{align*}
\]

Assume now that \( (a, c) \in s \), \( (b, e) \in s' \) and \( (a, b) \in fr \). Let us now prove that if \( s' \) is enforced, \( s \) is enforced too. Assume \( s' \) is enforced but \( s \) is not. Therefore, \( (c, b) \not\in syn \) but \( (c, a) \in syn \). We know that \( (a, b) \in fr \) and thus \( (a, b) \in syn \). By the transitivity property of \text{syn} we assert that since \( (c, a) \in syn \land (a, b) \in syn \) it must be that \( (c, b) \in syn \). This contradicts our assumption that \( s' \) is enforced. Therefore enforcing \( s' \) is sufficient to also enforce \( s \).

**End on \text{syn-type}**. Similarly, if \( s \) ends on a \text{syn-type} relation, we remove it to derive \( s' \). Assume the following example.

\[
\begin{align*}
s & \triangleq po_{wr}; fr; po_{wr}; fr \\
s' & \triangleq po_{wr}; fr; po_{wr}
\end{align*}
\]

Assume now that \( (a, c) \in s \), \( (a, b) \in s' \) and \( (b, c) \in fr \). Using the same proof as above, we can infer that if \( s' \) is enforced then \( (a, b) \notin syn \) and thus it follows that \( (c, a) \notin syn \). Therefore enforcing \( s' \) is sufficient to also enforce \( s \).

**A combination of the above (IRIW – Figure 1b)**. When a sync-pat falls into more than one of the above irregular categories, we combine the techniques discussed above. For instance, let \( sirw \) be the IRIW sync-pat of Figure 1b (discussed in the Introduction).

\[
s_{irw} \triangleq rf; po_{rr}; fr; rf; po_{rr}
\]

This is an irregular sync-pat, which both starts with a \text{syn-type} and includes a composition of consecutive \text{syn-type} relations. We use the rules above to derive \( s'_{irw} \triangleq po_{rr}; syn_{rr}; po_{rr} \) and assert that if \( s'_{irw} \) is enforced then \( s_{irw} \) is also enforced. To enforce \( s'_{irw} \) cond-1 requires the \text{prt-ordering} \( pr_{rr} \) and cond-2 requires the \text{sr-t-ordering} \( sr_{rr} \) which is also required by cond-3.

### 6 From \text{rt-orderings} to MCMs

So far we have created a mapping from MCMs to \text{rt-orderings}, by establishing the sufficient \text{rt-orderings} to enforce any sync-pat. In this section, we use this result to obtain the reverse mapping from \text{rt-orderings} to MCMs, focusing our discussion solely on regular sync-pats, seeing as the enforcement of irregular sync-pats is done by mapping them to regular ones. To obtain the mapping from \text{rt-orderings} to sync-pats, we reverse each of the three conditions, assuming that an operation can be of type \( m \) or \( n \) where \( m, n \in \{read, write\} \). Specifically, given a protocol that enforces a set of \text{prt-orderings} \( R_p \) and a set of \text{sr-t-orderings} \( R_s \), a sync-pat \( s \) is enforced when it abides by the following conditions:

- **Cond-1**: \( s \) can include a \text{po-type} relation \( po_{mn} \) if \( pr_{mn} \in R_p \).
7 From rt-orderings to Protocols

In previous sections we established the mappings between the sync-pats and the rt-orderings. In this section, we relate rt-orderings to some well-known protocol design techniques. We start with a brief discussion on the prt-orderings and then we focus on the srt-orderings.

7.1 Enforcing rt-orderings

Prt-orderings model the operation of the ROB specifying when the memory system can begin executing an operation. Upholding the prt-orderings is as simple as inspecting the state of the ROB. For instance, enforcing $prt_{wr}$ implies that the memory system cannot begin executing a read $r$ from process $p$, until every preceding write in the ROB is completed.

Srt-orderings models how the memory system executes reads and writes. Below we discuss two common techniques that can be used to enforce srt-orderings 1) overlap and 2) lockstep.

Overlap. The srt-ordering $srt_{mn}$ can be enforced simply by ensuring that operations of type $m$ must overlap with operations of type $n$ in a physical location. For instance, we can enforce $srt_{nr}$, by ensuring that a write is propagated to $x$ nodes and a read queries $y$ nodes, where $x + y > N$ and $N$ is the number of nodes. Alternatively, both types of operations can “meet” in some centralized physical location (e.g., the directory for multiprocessors). To ensure all four srt-orderings and thus linearizability, both reads and writes must query $y$ nodes to learn about completed operations and must broadcast their results to $x$ nodes. This is exactly how the multi-writer variant of ABD [14] operates.

Lockstep. Lockstep is a technique, where a memory system node first “grabs a lock” on the object before beginning an operation and releases it when the operation completes. Upon grabbing the lock, the node learns about the operation executed by the previous lock holder. The act of “grabbing the lock” is similar to getting a cache-line in a coherence protocol [17], or becoming the leader of the next log entry in a state machine replication protocol, such as Paxos [11]. Notably, lockstep entails overlap as operations must meet in a physical location to exchange the lock, but it also precludes the operations from executing concurrently.

There are two aspects of lockstep that can enforce srt-orderings. First, the srt-ordering between two operations is enforced if a lock must be passed from one to the other. For example we can enforce $srt_{rw}$ by mandating that a lock must be grabbed to perform a write. Second, locking also ensures that certain operations cannot overlap in real-time. When a write cannot overlap with a write and $srt_{rw}$ is enforced then $srt_{rw}$ is also enforced. This is because if a read $r$ returns the value of write $w$, then a write $k$ that begins after $r$ has completed must also begin after $w$ has completed. Similarly, when a write cannot overlap with a read and $srt_{wr}$...
is enforced, then \(srt_r\) is enforced. This is because if a read \(r\) returns the value of write \(w\), then it must be that \(w\) completes before \(r\) begins. Therefore, a read \(m\) that begins after \(r\) has completed, must also begin after \(w\) has completed and thus will observe \(w\). Protocols often combine the two aspects of lock-step to enforce the single-writer multiple-reader invariant (SWMR) [17], where for any given object at any given time there is either a single write in progress or multiple reads. This ensures that writes must grab a lock from each other \((srt_{rw})\), reads must grab a lock from writes \((srt_{rw})\), writes cannot overlap in time \((srt_{rw})\) and writes do not overlap in time with reads \((srt_r)\).

8 Discussion

In this work, we have used the rt-orderings to model the protocol, allowing us to create a mapping from MCMs to protocols. In this section, we discuss other use-cases of the rt-orderings. We start by describing the relation of srt-orderings to linearizability and then we discuss how they can be used to describe the real-time guarantees of existing protocols and to decide the consistency guarantees provided when protocols are composed.

8.1 Relation of srt-orderings to linearizability

Formally, the lin criterion [8] can be written in our notation as follows. An execution \(E(M, po, rf, hb, RL)\) is linearizable if there exists \(rl \in RL\) such that \(hb \subseteq rl\). Furthermore, because lin is a local property, it suffices that only operations to the same object abide by the rule. Plainly, for two operations \(a, b\) to the same object \(x\), if \((a, b) \in hb\) then it must be that \((a, b) \in rl\). This is equivalent to: \(acyclic(hb, syn)\). This, in turn, is equivalent to enforcing all four srt-orderings. Therefore, the lin property is the property of enforcing all four srt-orderings.

Intuition. Informally, the lin property can be defined by writing that each memory operation appears to take effect at some point between its invocation and completion [7]. Notably, each of the srt-orderings is a specialization of this definition. For instance, \(srt_{lat}\) mandates that each write appears to take effect at some point between its invocation and completion w.r.t. every read. Combining all four srt-orderings mandates that each write or read appears to take effect at some point between its invocation and completion w.r.t. every read or write. This is equivalent to the lin definition.

8.2 Srt-orderings for compositionality

So far we have viewed the srt-orderings solely as a mathematical model of the protocol. However, in distributed systems, it is often necessary to describe the real-time guarantees offered by a system, in order to compose different systems. Consider the example of Zookeeper. Zookeeper does not offer linearizability, and thus multiple Zookeeper instances cannot be composed. However, researchers have found that Zookeeper does offer some real-time guarantees that can be leveraged to achieve compositionality [12].

Srt-orderings can be used to capture these real-time guarantees. For example, the precise real-time guarantees of Zookeeper are the \(srt_{rw}\) and the \(srt_{rw}\) srt-orderingsand all four prt-orderings. More importantly, given this knowledge we can specify the MCM provided by composing different Zookeeper instances: the composed system will enforce the same rt-orderings as a single Zookeeper instance and thus we can use the reverse mapping from rt-orderings to sync-pats to specify the resulting MCM. In fact, we can use srt-orderings in the same spirit, to specify the MCM of any combination of composed systems, by asserting that the composed system will enforce any rt-ordering that is enforced by all of its subsystems.

9 Related Work

This work is the first to provide a mapping from MCMs to the protocols that can enforce them. To present this mapping we have used an abstract system model and the formalism presented by Alglave et al. [2] in order to describe MCMs, executions and real-time guarantees. Several works [4–6, 13, 20] have also described similar system models and formalism, but differ from our work in that they do not provide a mapping from MCMs to the protocols. Specifically, Szekeres and Zhang [20] provide a system model and a formalism called result visibility to describe consistency guarantees, including real-time guarantees. Crooks et al. [5], focusing on databases, provide a state-based formalization of isolation guarantees. Burckhardt, in his book on Eventual Consistency [4], provides a formalism to describe consistency models and protocols, with a focus on weaker guarantees. Levi-ari et al. [13] define Ordered Sequential Consistency, OSC(A), in order to specify the real-time guarantees of a protocol (with a focus on Zookeeper [9]). Similarly, Gotsman and Burckhardt propose GSC [6], a generic operational model for systems that totally order all writes, which can capture all of the srt-orderings for such systems.

In the cache coherence literature, the four program-orderings are used to describe consistency guarantees [17]. In fact, researchers have shown that when the coherence protocol enforces the single-writer multiple-reader (SWMR) invariant, the MCM depends solely on the enforced program orderings [3, 16]. Program orderings are very similar to prt-orderings with the subtle difference that program orderings carry the implication that the memory system enforces SWMR. In contrast, prt-orderings make no such assumption, allowing us to explore all possible behaviours of the memory system.

Finally, CCICheck [15] provides a way to verify an existing coherence protocol against its target MCM using the notion of µhb orderings, which are related to real-time. Our work
provides a mapping from MCMs to protocols, enabling the design of minimal protocols for any MCM.

10 Conclusion
In this work, we took an important step towards actualizing our overarching vision, which is the automation of the design of protocols that are responsible to enforce the consistency model (MCM) in shared memory systems. Specifically, we argued for the need of an intermediate abstraction between the MCM and the protocol implementation, that will allow us to map the MCM to specific protocol implementation techniques. We proposed such an abstraction by mathematically modelling the protocol through eight rt-orderings. To do so, we observed that any such protocol is comprised by two gadgets: the ROB and the memory system. We mathematically abstracted the ROB with the four prt-orderings and the memory system with the four srt-orderings. Crucially, we created a mapping from consistency guarantees to the rt-orderings, such that any MCM can be translated into the minimal set of rt-orderings that are required to enforce it. Finally, we completed the picture, by relating the rt-orderings to protocol implementation techniques, paving the way for automating protocol design.

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