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Integration of ZnO nanorods with MOS capacitor for self-powered force sensors and nanogenerators

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Abstract

In this work, we present a novel force-sensing device with zinc oxide nanorods (ZnO NRs) integrated with a metal-oxide-semiconductor (MOS) capacitor and encapsulated with Kapton tape. The details of the fabrication process and working principle of the integrated ZnO NRs-MOS capacitor as a force sensor and nanogenerator have been discussed. The fabricated ZnO-MOS device is tested for both the open-circuit and resistor-connected mode. For an input force in the range of 1–32 N, the open-circuit output voltage of the device is measured to be in the range of 60–100 mV for different device configurations. In the resistor-connected mode, the maximum output power of 0.6 pW is obtained with a 1 M Ω external resistor and input force of 8 N. In addition, the influence of different seed layers (Ag and ZnO) and the patterning geometry of the ZnO nanorods on the output voltage of ZnO-MOS device have been investigated by experiments. An equivalent circuit model of the device has been developed to study the influence of the geometry of ZnO NRs and Kapton tape on the ZnO-MOS device voltage output. This study could be an example of integrating piezoelectric nanomaterials on traditional electronic devices and could inspire novel designs and fabrication methods for nanoscale self-powered force sensors and nanogenerators.

Supplementary material for this article is available [online](#)

Keywords: self-powered force sensor, nanogenerator, ZnO nanorods, MOS capacitor, piezotronics

(Some figures may appear in colour only in the online journal)

1. Introduction

Since the initial work on the application of piezoelectric zinc oxide nanorods (ZnO NRs) for the conversion of mechanical energy into electrical energy in 2006 [1], the nanostructure-based piezoelectric devices have drawn a lot of interest in energy harvesting [1–3] and self-powered strain/stress sensing applications [4–7]. The working principle of these devices is based on the piezoelectric effect: the input mechanical stress

³ Deceased 15 July 2019.

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Figure 1. Device structure diagrams of (a), (b) ZnO NRs nanogenerators; (c) ZnO NRs piezo-gated force-sensing transistor; (d) ZnO NRs integrated on MOS capacitor.

results in induced polarization charges or electric field between the two terminals of piezoelectric materials [8]. The polarization charges or electric fields can be used either as a signal to external circuits or as an energy source to other devices. Therefore, the device based on the piezoelectric material can be self-powered and can work without an external power supply, which has attracted much attention in future cost-saving sensing applications [9, 10]. Specifically, for the piezoelectric semiconductors such as ZnO and gallium nitride (GaN), they could form Schottky barriers (SB) with contact metal such as gold (Au) or platinum (Pt) [11]. The piezoelectric polarization can be used to modulate the SB between the piezoelectric semiconductor and metal, which provides more possibility for novel sensing microsystems [4, 11–14].

To date, ZnO NRs-based devices have been studied mostly among all the nanostructure-based piezoelectric devices, mainly due to the promising properties and relatively simple synthesis procedures of ZnO NRs. Vertical ZnO NRs can be grown on various substrates by a wet chemical method called hydrothermal growth [15]. The hydrothermal growth mechanism of ZnO NRs and patterned growth method during the ZnO NRs-based device fabrication have been studied extensively by many researchers [16–20]. Many different ZnO NRs-based high-performance novel nanogenerators and force sensors have been achieved [21–31]. For example, figure 1(a) shows the typical structure of a vertical ZnO NRs-based nanogenerator. As can be seen, metal is in direct contacted with both ends of the ZnO NRs, and the polymers such as polymethyl methacrylate, polydimethylsiloxane, and polyimide (PI) are used to encapsulate the ZnO NRs [7, 24, 25]. However, in real fabrication cases, it is relatively difficult to control the etching of polymer precisely to expose the ZnO NRs and then metallize directly on the top of ZnO NRs. Therefore, many researchers have presented a nanogenerator structure with polymer between the top-side of NRs and top metal contact [26–28], which is shown in figure 1(b). However, the polymer related capacitance between the top and bottom metal contact could have an influence on the output voltage. Moreover, in the literature,

Figure 2. (a) Structure of the ZnO-MOS device; (b) top-view of ZnO-MOS device without encapsulation; (c) Al-foil contact, encapsulation, and testing of ZnO-MOS.

researchers have designed vertical ZnO NRs as gate control on a field-effect transistor, as shown in figure 1(c). The transistor channels have been achieved by doped silicon [29] or two-dimensional (2D) materials such as graphene [30] and 2D molybdenum disulfides [31]. In these force-sensing transistors, the ZnO NRs have only one end connected to the top of the transistor channel; and the polymer could also be used for the top-side encapsulation of ZnO NRs. However, the investigation on the top ZnO NRs-polymer piezo-gated control is still limited in the literature.

Our work here presents an integrated structure of ZnO NRs on a traditional metal-oxide-semiconductor capacitor (ZnO-MOS), as shown in figure 1(d). The capacitance of the MOS capacitor could be designed by the geometry of the device structure. Kapton tape (polyimide film) has been used to encapsulate the device. Instead of top-side metallization for the device, a metal probe is used to apply the force. The detailed force-sensing mechanism of ZnO-MOS device has been discussed. In addition, the influence of the different seed layers for the growth of ZnO NRs and the geometry of ZnO NRs patterning area on the electrical output has been studied experimentally. An equivalent circuit has been modelled to study the influence of the geometry of ZnO NRs and Kapton tape on the ZnO-MOS device voltage output. Overall, the aim of this work is (a) to investigate the mechanism of piezoelectric material-polymer hybrid structure, which could possibly be used as the gate control building block of the transistor; (b) to develop a novel device-level design for using piezoelectric nanomaterial in applications including human-robotic interface, biomimetic skin, and internet of things (IoT).

2. Materials and methods

Figure 2 shows the overall device structure of the integrated ZnO NRs-MOS capacitor. The detailed microfabrication process flow has been presented in figure S1 (available online at stacks.iop.org/NANO/32/455502/mmedia) of the supplementary information. Double-side polished 3 inch Si wafers doped by boron (p-type heavily doped), with a resistivity of 0.001–0.005 Ω cm, have been used as the substrate for the devices. 300 nm SiO_2 has been grown on both sides by

dry oxidation. The oxide on the backside of the wafer has been removed by buffered hydrofluoric acid wet etching, following by sputtering of 100 nm Ti on the backside. For the top-side, 100 nm thick Ti has been patterned by photolithography and deposited by sputtering. The top Ti square's patterned geometry has been designed as 5 mm width squares, which contributes to a capacitance of ~ 2.88 nF. Then, 200 nm aluminium (Al) has been deposited on the side of the Ti square as a grid for the electrode contact.

Two different types of seed layers, 50 nm Ag and 50 nm ZnO thin-films, have been patterned as a 4 mm width square by photolithography and deposited by e-beam evaporation. Afterwards, three kinds of areas with different patterned geometries (with ZnO NRs growth area decreasing by a factor of 5) have been defined by photolithography: 1 mm width squares (only patterned with a large area, called non-patterned in the following), $10\ \mu\text{m}$ lines with a distance of $40\ \mu\text{m}$ (lines array), and small squares array of $10\ \mu\text{m}$ width with $40\ \mu\text{m}$ distance (squares array). In the following, the hydrothermal growth of ZnO NRs has been performed. The sample wafers have been put top-side down and floated in 250 ml DI water with 40 mM 1:1 zinc nitrate hexahydrate [$\text{Zn}(\text{NO}_3)_2 \cdot 6\text{H}_2\text{O}$] and HMTA (hexamethylenetetramine) precursors. ZnO NRs have been grown at $90\ ^\circ\text{C}$ for 18 h. After hydrothermal growth of ZnO NRs, Acetone has been used to strip the photoresist which is used to define the area for ZnO NRs. Scanning electron microscopy (SEM) have been used to characterize the length/diameter/density of the patterned ZnO NRs.

Before the encapsulation, 3 inch wafers have been diced into $1\ \text{mm}^2$ chips. Al-foil and Ag adhesion have been used to connect with the top and bottom Ti electrode, followed by encapsulation of $\sim 70\ \mu\text{m}$ thick Kapton tape. It is worth noting that, due to the influence of Al-foil, the capacitance of the overall MOS capacitor could be slightly larger than the designed value, which is measured typically at around 3 nF. For the testing, conducting foils have been connected to the Keithley 4200 semiconductor analyzer. Then the force gauge (Mark-10 ESM 303 Force Tester) with a metal probe of $1\ \text{mm} \times 5\ \text{mm}$ has been used to apply force on the ZnO NRs without touching on the Al foils area. A more detailed experimental setup has been presented in figure S2 of the supplementary information. Moreover, an equivalent circuit is modelled in MATLAB, and correlated with the experimental results.

3. Results and discussion

3.1. Working mechanism

Figure 3(a) shows the working diagram when different forces are applied to the ZnO-MOS devices. Taking the Ag seeded non-patterned ZnO NRs sample as an example, both the open-circuit mode and the resistor-connected mode have been tested. Firstly, the bottom contact of the MOS capacitor is connected to the ground, and the electric potential of the top electrode is tested. An input force in the range of 1–32 N is applied on the device by the metal probe. The force could be

Figure 3. (a) The diagram of working modes of the ZnO-MOS devices; (b) energy diagram of ZnO-Ag hetero-junction; open-circuit voltage output of the ZnO-MOS with; (c) steady force from 1 to 32 N, (d) 8 N pulse force with a frequency at around 0.5 Hz; (e) voltage drop in the connected resistor when 8 N force loading and releasing; (f) voltage change and total charge in the MOS capacitor as a function of applied force.

loaded in either steady force mode or pulse force mode with frequency at around 0.5 Hz; the results have been shown in figures 3(c) and (d), respectively. Figure 3(c) shows that the output voltage change on the Ag seeded non-patterned ZnO NRs sample is up to around positive 100 mV with the input force of 32 N, which is significantly larger than the output of the sample without ZnO NRs (~ 10 mV). The results in figure 3(d) show that the voltage change is relatively stable during the repeated loading and releasing with the same force. It worth noting that, after a certain time (~ 150 s), the voltage output became less stable, which is probably related to the strain-stress hysteresis due to the existence of the Kapton tape and the unstable mechanical coupling between Kapton tape and ZnO NRs. In addition to open-circuit characterization, the device is connected to a resistor with a resistance of $1\ \text{M}\Omega$. The voltage between two ends of the resistor has been measured for an input force of 8 N, as shown in figure 3(e). A positive voltage spike drop in the resistor is observed up to 0.5 mV, which is equivalent to a pulse current of a 0.5 nA peak (pulse width ~ 5 s) flowing in the resistor for the input force of 8 N. When the metal probe releases, a negative voltage spike drop in the resistor has been observed. The resistor-connected mode results show the potential of the

ZnO-MOS capacitor as a nanogenerator, which has a maximum power of around 0.6 pW for the ZnO-MOS device presented here. Moreover, the voltage output of the ZnO-MOS devices as a function of input force has been plotted and presented in figure 3(f). It can be seen that, even with 1 N input force, the voltage output can reach around 50 mV. As the input force increases from 1 to 10 N, the output voltage increases from 50 to 80 mV with a decreasing slope. For the input force larger than 10 N, the voltage output has been observed to increase linearly with force increasing, the sensitivity (voltage output/input force) has been estimated to be around 1.1 mV N^{-1} for the Ag seeded non-patterned ZnO NRs sample.

3.1.1. MOS capacitor. As shown in figure 3(a), ZnO NRs could be treated as a charge source that can charge up the MOS capacitor. If the device is open-circuited, the voltage change on the MOS capacitor is related to the overall charge ΔQ from ZnO NRs ($\Delta V = \Delta Q/C_{\text{MOS}}$), where C_{MOS} is the capacitance of the MOS capacitor. The capacitance of the MOS capacitor is determined mainly by the area (A) of the top Ti contact and thickness of SiO_2 (t_{ox}): $C_{\text{MOS}} = \epsilon_0 \epsilon_{\text{ox}} A/t_{\text{ox}}$, where ϵ_0 is the vacuum permittivity ($8.85 \times 10^{-12} \text{ F m}^{-1}$). The permittivity of SiO_2 (ϵ_{ox}) is around 3.9. Therefore, for our designed geometry of MOS capacitor (Ti: $5 \text{ mm} \times 5 \text{ mm}$, $t_{\text{ox}} = 300 \text{ nm}$), the capacitance should be 2.88 nF. Due to the heavily p-type doped Si, the threshold voltage (from depletion to inversion mode) of the MOS capacitor is high that results in a very stable capacitance that is slightly smaller than the designed value if only a small voltage is applied. However, the Al-foil used to connect the MOS capacitor to the external circuit may increase the contact area and thus increase the capacitance. The measured MOS capacitance for the device is typically at around 3 nF. It is worth noting that in figure 3(c), an off-set voltage has been observed in open-circuit mode, which is probably due to the residue charges stored in the MOS capacitor. These residue charges could be related to the charge accumulating on the surface of Kapton tape due to previous testing or possibly the native charge residues in the Si-SiO₂ interface due to the lattice defects [32]. To eliminate the off-set voltage, all the voltage curves in the following sections are normalized.

3.1.2. Charge transfer mechanism. To investigate the transfer mechanism of charge ΔQ from ZnO NRs to the MOS capacitor under the influence of an applied force, the energy diagram of the ZnO-Ag sample has been drawn in figure 3(b). ZnO NRs have been reported to be n-type doped due to the oxygen-related defects, which leads to a work function typically at around 5.3 eV [33]. The electron affinity of ZnO NRs has been assumed to be 4.5 eV [1], which is higher than the work functions of both Ag (4.26 eV [34]) and Ti (4.33 eV [35]). Therefore, the energy diagram shows no SB for the Ag-ZnO junction (also for the Ti-ZnO), and electrons can flow through the metal-semiconductor junction. When the force is applied to the ZnO NRs in the vertical direction, due to the piezoelectric effect of ZnO NRs in the

z-axis, a positive potential could be formed from the bottom of ZnO NRs to the floated top-end of ZnO NRs [1, 26]. Theoretically, there could be a drop of Fermi-level on the ZnO NRs side of the ZnO-Ag junction, together with a lower band bending of ZnO because of the floated top ZnO NRs end, as shown in the red line in figure 3(b). Therefore, there could be electrons flowing from Ag to the ZnO NRs. The transportation of negative charge from Ag to ZnO is equivalent to positive voltage change on the top of the MOS capacitor, in line with the results presented in figures 3(c)-(e).

3.1.3. Origin of charge. The total charge ΔQ on the top-side of the MOS capacitor, as a function of force has been calculated and shown in figure 3(f). In our previous explanation, the total charge ΔQ is assumed only due to the piezoelectric effect of ZnO NRs when force is applied. A device without ZnO NRs, which is only a MOS capacitor with the same encapsulation of Kapton tape, has also been tested as a reference to investigate the origin of charge. The voltage output of the no NRs device is significantly lower than Ag seeded ZnO NRs sample, and the polarization of voltage as different forces applied are different, which could be seen in figures 3(c) and (f). This observation indicates that the developed charge is mainly due to the presence of ZnO NRs.

However, for the no ZnO NRs device, there is still a signal change of up to 10 mV with different polarization, which should not be ignored as noise. There could probably be a few reasons to explain the output of no ZnO NRs devices: firstly, as the frequently reported triboelectric effect in the literature [36], when the metal probe is in contact with the Kapton tape, the Kapton tape might slide on the top metal contact in the lateral direction. Charges could be generated due to the contact and friction between different materials. The existence of contacting and friction charge could also explain the relatively high output voltage (50 mV) even with force lower than 1 N of the Ag seeded non-patterned ZnO NRs sample. Secondly, when the metal probe is in contact with the top of Kapton tape (polyimide, 70 μm thick), there might be a weak capacitive coupling between the top metal probe and the polyimide as the dielectric. The compression of polyimide could increase the capacitance between the metal probe and top metal contact of the MOS capacitor and hence change the charge distribution. Moreover, boron-doped Si has been reported to be piezoresistive [37], leading to a different charge distribution in the interface between the SiO₂ and Si when a force is applied. The overall charge change ΔQ could possibly be a combination of all these factors; however, we will focus on the role of the piezoelectric effect of ZnO NRs in the following section.

3.2. The influence of the type of seed layer and patterned geometry on the output voltage

In the literature, both the seed layer and the patterned geometry could be factors that have an influence on the performance of ZnO NWs piezoelectric devices [38, 39]. To further investigate these factors that could modify the output signal

Figure 4. (a) Squares and lines patterned geometry of ZnO NRs grown on Ag and ZnO seed layer. (b) 45° tiled SEM images of ZnO NRs and their voltage output, respectively. (c) The overall generated charges as a function of applied force.

from ZnO NRs, samples with different seed layers and patterned geometry have been fabricated and tested. Both Ag thin-film and ZnO thin-film have been used as the seed layers. For both Ag and ZnO seed layers, three different patterned geometries have been fabricated by photolithography, including squares patterned, lines patterned, and non-patterned. The SEM images of squares and lines patterned geometries have been shown in figure 4(a). The SEM images of ZnO NRs and open-circuit voltage output of all samples have been listed in figure 4(b), and the overall generated charge as a function of applied force has been plotted in figure 4(c). In addition, the detailed information on the influence of the parameters of ZnO NRs, such as diameter, length, and density of ZnO NRs, on the devices' output voltage has presented in table S1 of the supplementary information.

3.2.1. The influence of seed layer type on voltage output.

Firstly, different seed layer types have been observed to contribute to different diameters, lengths, and densities of ZnO NRs. As can be seen in figure 4(b) and the data in table S1 in the supplementary information, the ZnO NRs grown on Ag seed layer (length $\sim 7 \mu\text{m}$, diameter $\sim 700 \text{ nm}$ and density $\sim 100 \text{ NRs}$ in $10 \mu\text{m} \times 10 \mu\text{m}$) shows a significantly larger size and lower density than ZnO seeded ZnO NRs (length $\sim 4 \mu\text{m}$, diameter $\sim 170 \text{ nm}$ and density $\sim 1500 \text{ NRs}$ in $10 \mu\text{m} \times 10 \mu\text{m}$). The different growth characteristics of ZnO NRs have been reported to be a result of the different

seeding mechanisms from the different seed layers [16, 17]. The nucleation barrier between ZnO NRs and ZnO thin-film is less than the hetero nucleation barrier between Ag and ZnO, which results in a stronger seeding effect of ZnO seed layer on ZnO NRs than Ag seed layer.

From the literature, ZnO NRs with higher aspect ratios (length/diameter) can result in higher piezoelectric output [25]. In our experiment, ZnO seeded ZnO NRs (aspect ratio ~ 25) have a significantly higher aspect ratio than Ag seeded ZnO NRs (aspect ratio ~ 10). However, as can be seen in figures 4(b) and (c), the device output of ZnO seeded ZnO NRs has been observed to be always lower than Ag seeded NRs. Especially for the lines patterned and squares patterned ZnO seeded ZnO NRs, the output has been observed to be very low (less than 20 mV), which is almost similar to the sample without ZnO NRs (figure 3(c)). This observation could indicate the important role that the different seed layers play on the charge transport and hence on the device output. The fact that ZnO NRs with a lower aspect ratio give a larger output voltage suggests that there could be less charge transfer between ZnO NRs and Ti due to the semiconducting characteristics of the ZnO seed layer, and therefore, the lower voltage output of the device.

More generally, many other types of seed layers could also be used to grow ZnO NRs, such as Au [40] and GaN [41]. The different seed layers may result in different dimensions of ZnO NRs, and therefore different piezoelectric output. However, the

influence of the seed layer on the charge transfer may also contribute to the voltage output. In addition, more complicated interface cases between ZnO NRs and seed layer have been reported, such as the SB (Au–ZnO) [11], and the existence of different semiconductor hetero-junction due to different doping levels (ZnO–GaN) [42].

3.2.2. The influence of patterned geometry on voltage output.

Firstly, the length/diameter/density of ZnO NRs have been observed to show a dependence on patterned geometries. For the same seed layer, as the ZnO NRs patterned area decreases from non-patterned to squares and lines patterned, both the diameter and length of ZnO NRs have been observed to increase, and the density has been observed to decrease. Thus, the aspect ratio of NRs on both squares patterned and lines patterned samples has been observed to be slightly higher than non-patterned samples. The reason could be that the patterned geometry could affect the mass transportation during the hydrothermal growth, thus leading to the different precursors' concentrations in different regions, and eventually resulting in different growth characteristics of ZnO NRs [19].

For the voltage output results (figures 4(b) and (c)), the overall trend is that the non-patterned sample has a larger voltage output than lines patterned and squares patterned sample for both Ag and ZnO seeded layers. The voltage output of the difference between lines patterned sample and squares patterned sample is insignificant. Especially for Ag seeded ZnO NRs, the voltage output of lines patterned sample is very close to the squares patterned sample, as shown in figure 4(b). These observations do not follow the expected trend that the higher aspect ratio of ZnO NRs with the higher voltage output [25]. A possible reason could be the non-uniform force or pressure distribution due to different ZnO NRs patterned geometry. The Kapton tape in the surroundings of ZnO NRs may have an effect on the device output by sharing the induced strain.

Overall, the effect of the different seed layers and patterned geometry will both result in NRs with different lengths, diameters and densities. However, if only based on the samples in our experiments, the influence of the length, diameter and density of ZnO NRs on the voltage output is unclear, while the voltage output of the devices shows more dependence on the type of seed layer and the patterned area of ZnO NRs. The different voltage output of different devices could be explained by the effective charge transfer between the ZnO seed layer and Ag seed layer, and the force distribution due to the patterned geometry and the Kapton tape. To further investigate the parameters that could influence the voltage output, modelling and simulation has been performed and presented in the following sections, which will include the study of the length, the overall coverage area of ZnO NRs, and the geometry of Kapton tape on the device output.

3.3. Equivalent circuit and modelling

To further investigate the working mechanism of the ZnO-MOS device, an equivalent circuit model has been built, which is shown in figure 5(a), and the overall schematic for

the modelling has been presented in figure 5(b). The metal probe has been assumed to be grounded when the force is loaded. In addition, ZnO NRs are assumed to be aligned perfectly in the [0001] direction, and only the direct piezoelectric effect is considered. The overall working equations for the ZnO-MOS device are shown in the following:

$$F_{\text{ZnO}} = F_{\text{overall}} - F_{\text{Kapton_side}}, \quad (1)$$

$$Q_{\text{piezo}} = F_{\text{ZnO}} d_{33}, \quad (2)$$

$$q = \frac{Q_{\text{piezo}}}{\frac{C_{\text{ZnO}}}{C_{\text{Mos}} + C_{\text{Kapton_side}}} + \frac{C_{\text{ZnO}}}{C_{\text{Kapton_top}}} + 1}, \quad (3)$$

$$V_o = \frac{q}{C_{\text{MOS}} + C_{\text{Kapton_side}}}, \quad (4)$$

where F_{overall} , F_{ZnO} , $F_{\text{Kapton_side}}$ are the overall force applied on the ZnO-MOS device, the force on ZnO NRs, and the force on the Kapton tape in the surroundings of ZnO NRs, respectively. The d_{33} is the effective piezoelectric constant for ZnO in the [0001] direction, which is reported to be in the range of 9.93–26.7 pC N⁻¹ [43]. The Q_{piezo} is the piezoelectric charge generated by ZnO NRs, q and V_o are the charges transferred from ZnO NRs to the MOS capacitor and voltage output of the device, respectively. The following equations show the expressions for the capacitance of the ZnO and Kapton tape (polyimide):

$$C_{\text{ZnO}} = \varepsilon_0 \varepsilon_{\text{ZnO}} A_{\text{ZnO}} / L_{\text{ZnO(F)}}, \quad (5)$$

$$C_{\text{Kapton_top}} = \varepsilon_0 \varepsilon_{\text{PI}} A_{\text{ZnO}} / t_{\text{Kapton(F)}}, \quad (6)$$

$$C_{\text{Kapton_side}} = \varepsilon_0 \varepsilon_{\text{PI}} A_{\text{Kapton_side}} / t_{\text{Kapton(F)}}, \quad (7)$$

where ε_{ZnO} and ε_{PI} are the relative dielectric constant of ZnO and polyimide with a value of 8.5 [44] and 3.4 [45], respectively. A_{ZnO} , L_{ZnO} , t_{Kapton} are the total coverage area of ZnO NRs connected with other parts, the length of ZnO NRs, and the thickness of Kapton tape, respectively. The area of Kapton tape on the side of ZnO NRs is represented as $A_{\text{Kapton_side}}$. The $L_{\text{ZnO(F)}}$ and $t_{\text{Kapton(F)}}$ have been defined as the length of ZnO NRs, and the thickness of Kapton tape after the force is applied, respectively. The value of $L_{\text{ZnO(F)}}$ and $t_{\text{Kapton(F)}}$ is smaller than the initial value ($L_{\text{ZnO(0)}}$ and $t_{\text{Kapton(0)}}$) due to the presence of the stress and can be written as:

$$L_{\text{ZnO(F)}} = L_{\text{ZnO(0)}} - \frac{L_{\text{ZnO(0)}} F_{\text{ZnO}}}{A_{\text{ZnO}} Y_{\text{ZnO}}}, \quad (8)$$

$$t_{\text{Kapton(F)}} = t_{\text{Kapton(0)}} - \frac{t_{\text{Kapton(0)}} F_{\text{overall}}}{A_{\text{probe}} Y_{\text{PI}}}, \quad (9)$$

where Y_{ZnO} and Y_{PI} are the Youngs' modulus of ZnO and polyimide with a value of 140 GPa [46] and 3 GPa [45], respectively.

3.3.1. Modelling of voltage output. The voltage output as a function of applied force has been shown in figure 5(c). Both models with the piezoelectric coefficient of 9.93 and 26.7 pC N⁻¹ have been plotted. The A_{ZnO} , L_{ZnO} , and t_{Kapton} have been fixed at a value of 0.29 mm², 10 μm, and 70 μm, respectively, which is based on the geometry of the fabricated device (Ag seeded non-patterned sample). The area of Kapton tape on the side of ZnO

Figure 5. (a) Equivalent circuit for ZnO-MOS capacitor model; (b) modelling schematic and parametric studies. (c) Voltage output from modelling and experiment with the input force ranging from 0 to 35 N; the modelled voltage output with an input force of 20 N, as a function of: (d) overall coverage area of ZnO NRs (A_{ZnO}); (e) initial length of ZnO NRs ($L_{\text{ZnO}(0)}$); (f) initial thickness of Kapton tape on top ($t_{\text{Kapton}(0)}$); and (g) ratio of area of Kapton tape on the side to ZnO NRs ($A_{\text{Kapton_side}}/A_{\text{ZnO}}$).

has been fixed at zero, which means all the force has been assumed to be applied on ZnO NRs, as shown in equation (1).

As shown in figure 5(c), the modelled voltage output has a linear relationship with the applied force, which is consistent with equations (1)–(4). For an input force of 30 N, the voltage output is around 10–20 mV. The slope of modelled voltage output has been observed to be similar to the experimental output voltage slope of the device in the input force range between 20 and 30 N. It could be speculated that the d_{33} value of the experimental device is of the same order of magnitude as the reported value ($9.93\text{--}26.7 \text{ pC N}^{-1}$). However, the results in figure 5(c) show that the modelled voltage output of the device is significantly lower than the experimental result, and the experimental result is nonlinear for the input force up to 10 N. A possible reason for this difference could be the charge accumulated at the top of Kapton tape, due to the contacting and friction between the metal probe and the top surface of Kapton tape, when the metal probe is loaded on the device initially.

3.3.2. Influence of ZnO NRs' geometry on the voltage output.

In our device, since the ZnO is not a continuous and uniform thin-film but an array of NRs, the A_{ZnO} is the real contacting area (top-side) of ZnO NRs with Kapton tape. The A_{ZnO} is

related to the designed growth area, the density and the diameter of ZnO NRs. For the Ag seeded ZnO NRs non-patterned sample, the A_{ZnO} has been measured to be around 0.29 mm^2 from SEM images ($\sim 29\%$ NRs area coverage for $1 \text{ mm} \times 1 \text{ mm}$ designed ZnO NRs area).

The influence of the A_{ZnO} and initial length of ZnO NRs $L_{\text{ZnO}(0)}$ on the device output voltage have been studied and presented in figures 5(d) and (e), respectively. The results show that as the A_{ZnO} increases, the output voltage decreases and becomes saturated at an area of around 0.02 mm^2 , while the output voltage increases linearly with the increase of $L_{\text{ZnO}(0)}$. Thus, in the developed circuit mode, the trend that the higher the aspect ratio of ZnO NRs, the higher the voltage output is evident. It can also be seen that the length of the ZnO NRs has a stronger influence compared to the area of the NRs. The correlation among A_{ZnO} and $L_{\text{ZnO}(0)}$ on the voltage output can be explained by the change of the capacitance of the ZnO NRs (C_{ZnO}). The smaller A_{ZnO} and the larger $L_{\text{ZnO}(0)}$ result in a smaller C_{ZnO} (equation (5)), and hence more charge (q) is transferred to the MOS capacitor (equation (3)) and voltage output increases (equation (4)).

From figure 5(d), it is evident that the magnitude of voltage output saturates at around 10 mV when A_{ZnO} is above 0.02 mm^2 . The explanation could be that when the A_{ZnO} is

relatively large, the typical value of C_{ZnO} (~ 1 pF) is negligible in comparison to C_{MOS} (3 nF). Hence, the term $C_{\text{ZnO}}/C_{\text{MOS}}$ is negligible. In addition, in the term $C_{\text{ZnO}}/C_{\text{Kapton_top}}$, the A_{ZnO} could be cancelled out, and thus, the influence of A_{ZnO} on the voltage output is limited. However, when the A_{ZnO} is very small, in our case below 0.02 mm^2 , the transient length of ZnO NRs ($L_{\text{ZnO(F)}}$) can show a noticeable dependence on the A_{ZnO} when the same force is loaded (equation (8)). In other words, if the area of ZnO NRs is very small, the stress or deformation of ZnO NRs in the vertical direction can not be ignored. In this case, the influence of A_{ZnO} on the ratio $C_{\text{ZnO}}/C_{\text{Kapton_top}}$ could not be ignored, and the voltage output could show an apparent correlation with the A_{ZnO} . For almost all of experimental samples, the calculated overall coverage area is larger than 0.02 mm^2 (supplementary information, table S1), the influence of the patterned area on voltage output could be limited; therefore, the diameter and density of ZnO NRs could have a limited effect on the voltage output in our devices.

3.3.3. Influence of the Kapton tape on voltage output. As could be seen in the equivalent circuit (figure 5(a)), the Kapton tape has been separated into two parts, the Kapton tape directly on the top of ZnO NRs, and the Kapton tape on the side of ZnO NRs.

The dependence of voltage output on the initial thickness of Kapton tape on top of ZnO NRs have been studied and shown in figure 5(f). As can be seen, the thicker the Kapton tape on top of ZnO NRs, the lower the voltage output. Based on equations (3) and (6), the Kapton tape directly on the top of ZnO NRs could influence the capacitance ratio $C_{\text{ZnO}}/C_{\text{Kapton_top}}$, and hence change the charge (q) from ZnO NRs to the MOS capacitor. The typical value of $C_{\text{Kapton_top}}$ is around 0.05 pF if the thickness of Kapton is fixed at $70 \text{ }\mu\text{m}$, the capacitance of which is ~ 20 times smaller than C_{ZnO} . Therefore, according to equation (3), the Kapton tape on top of ZnO NRs could have a significant influence in scaling down the voltage output. Therefore, more generally, for the ZnO-MOS device, a thinner polymer encapsulation is suggested for higher voltage output.

For the Kapton tape on the side of ZnO NRs, the capacitor $C_{\text{Kapton_side}}$ (less than 1 pF) is significantly smaller than the C_{MOS} (~ 3 nF). Based on equation (3), the influence of $C_{\text{Kapton_side}}$ could be negligible to the overall output. However, as can be seen in equation (1), the Kapton on the side could share the force or strain with ZnO NRs. In the actual device, it is a challenge to measure the area of Kapton tape on the side of ZnO NRs. During the simulation, a simplified model for force distribution has been used, which assumes that ZnO NRs are in parallel with the Kapton on the side, and the ZnO NRs's length is negligible in comparison to the Kapton tape's thickness. In this case, the stress of Kapton tape should be the same as the ZnO NRs together with the Kapton tape on top, therefore:

$$\frac{F_{\text{Kapton_side}}}{Y_{\text{PI}}A_{\text{Kapton_side}}} = \frac{F_{\text{ZnO}}}{Y_{\text{PI}}A_{\text{ZnO}}} + \frac{F_{\text{ZnO}}}{Y_{\text{ZnO}}A_{\text{ZnO}}}. \quad (10)$$

As shown in equation (10), the force on ZnO NRs and the force shared by the Kapton tape $F_{\text{Kapton_side}}$ depends on the area

ratio ($A_{\text{Kapton_side}}/A_{\text{ZnO}}$). Combined with equations (1)–(4), the relationship between the area ratio ($A_{\text{Kapton_side}}/A_{\text{ZnO}}$) and voltage output has been shown in figure 5(g). As can be seen, as the area ratio $A_{\text{Kapton_side}}/A_{\text{ZnO}}$ increases, the output voltage decreases, and when this ratio is higher than 10, the output voltage saturates. The result of equivalent circuit modelling agrees with the experimental result that non-patterned sample has significantly higher output voltage than lines patterned, and squares patterned samples, although ZnO NRs of the non-patterned samples have a lower aspect ratio than patterned samples. These observations indicate the important role the Kapton on the side of ZnO NRs play on the force distribution, hence on the device's voltage output.

4. Conclusion

In conclusion, we have demonstrated the integrated structure of ZnO NRs on a MOS capacitor (ZnO-MOS) as a force sensor or a nanogenerator. Only the bottom side of ZnO NRs has been connected with the top metal contact of the MOS capacitor; the top-side of ZnO NRs is floated and encapsulated with the Kapton tape. For the non-patterned Ag seeded ZnO NRs, the voltage output of the MOS capacitor has been found to be 60–100 mV when the applied force is in the range 1–32 N. and up to 0.6 pW maximum power have been observed when the device is connected with a $1 \text{ M}\Omega$ resistor.

The influence of the seed layer and patterned geometry on the voltage output has been studied experimentally. The device samples with Ag seeded ZnO NRs show a higher voltage output than those with ZnO seeded ZnO NRs. The voltage output of non-patterned samples has been observed to be higher than lines and squares patterned samples.

Numerical modelling has been performed on the ZnO-MOS device. The results demonstrated that the longer length of ZnO NRs contributes to the higher voltage output, while the overall coverage area of ZnO NRs has a limited influence on voltage output. The model also shows that the thinner the Kapton tape thickness and the smaller the area of the Kapton tape on the side of the ZnO NRs, the higher will be the output voltage of the device.

The output of this work could provide a technical route for the design and fabrication of piezoelectric nanorods without top-side metallization, which could be applied in the strain/stress gate control transistor, controllable nanogenerator and self-powered nanoscale force sensors in future human-machine interface and IoT systems.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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