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The Piezoelectronic Stress Transduction Switch for VLSI, low voltage sensor computation, and RF applications

I.-B. Magdău[1,2], X.-H. Liu[3], M.A. Kuroda[4], T.M. Shaw[3], J. Crain[1,2], P.M. Solomon[3], D.M. Newns[5], and G.J. Martyna[1,5]

1. School of Physics of Astronomy, University of Edinburgh, Edinburgh, UK.
2. National Physical Laboratory, Teddington, UK.
3. Silicon Technology, IBM TJ Watson Research Center, Yorktown Heights, NY USA.
4. Department of Physics, Auburn University, Auburn, AL USA.
5. Physical Sciences, IBM TJ Watson Research Center, Yorktown Heights, NY USA.

Abstract: The piezoelectronic transduction switch is a novel device with high potential as a post–CMOS transistor due to its predicted multi-GHz, low voltage performance on the VLSI-scale. However, the operating principle of the switch has much wider applicability. We use theory and simulation to optimize the device across a wide range of length scales and application spaces and to understand the physics underlying its behavior. We show that the four-terminal VLSI-scale switch can operate at a line voltage of 115 mV while as a low voltage- large area device, ≈200 mV operation at clocks speeds of ≈2 GHz can be achieved with a desirable 10^4 On/Off ratio - ideal for on–board computing in sensors. At yet larger scales, the device is predicted to operate as a fast (≈250 ps) RF switch exhibiting high cyclability, low On resistance and low Off capacitance, resulting in a robust switch with a RF figure of merit of ≈4 fs. These performance benchmarks cannot be approached with CMOS which has reached fundamental limits. A combination of finite element modeling and *ab initio* calculations enables prediction of switching voltages for a given design. A multivariate search method then establishes a set of physics-based design rules, discovering the key factors for each application. The results demonstrate that the piezoelectronic transduction switch can offer fast, low power applications spanning several domains of the information technology infrastructure.

Main: We are entering a new era in information technology (IT) where a rapidly increasing number of interconnected devices at various scales, is driving corresponding increases in both data volume, and the energy to process, archive and/or communicate it. Indeed, the worlds's data centers, cell phones, laptops, tablets, etc., may now draw as much as 10% of the world's electrical power production [1]. Remediation by reducing energy/bit is no longer a viable strategy because the current computer technology, CMOS, has reached fundamental limits which prevent further Dennard (voltage) down-scaling with chip generation [2]. This has led to a power bottleneck [3-5] - although the Moore's law shrink will continue for a few more generations [3]. The development of novel architectures based on different physical principles, capable of populating critical applications spaces with *fast, low power* solutions, has therefore become crucial to support the evolution of IT into the mega-data era.

Recently, we have invented a new technology, the PiezoElectronic Transistor (PET), shown in its 4-terminal form in Fig. 1, modeled its performance in the VLSI space as a fast, low power 3-terminal device [6-8], and fabricated several prototypes demonstrating proof of principle [9,10]. The PET is potentially both low power and fast because of its stress transduction operating principle: A voltage signal arrives, charging a piezoelectric (PE) capacitor [11,12], which expands,

compressing a piezoresistive (PR) channel material [13,14] against a rigid surrounding yoke/frame, transducing the input signal into internal stress. The PR undergoes a continuous insulator to metal transition with applied stress, turning the device On and thereby transducing the internal stress into an output voltage signal. The transduction of the input voltage to an internal stress state of the PET device means that the current through the channel is controlled by the stress-dependent resistivity of the PR. This is in contrast to the electrostatic control mechanism utilized by CMOS [2-5] which can no longer scale down voltage and power with generation. PET performance relies on the integration of PR and PE materials such as SmSe or $Sm_xEu_{1-x}S$ [13-14] and as $Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMN-PT) [11-12,15] into structures such as Fig. 1. Speed is controlled by matching the RC time ($R_{\mathrm{On}}^{(\mathrm{PR})}C^{(\mathrm{PE})}$) and sound crossing time (PE height / PE speed of sound) which can easily reach picoseconds. These results together with FEM simulations show that a VLSI-scale PET device can attain a resistive On/Off ratio of 10^4 at gate voltages of order 0.1 V, while operating at 10 GHz [6,7,16] - provided near bulk properties of the materials SmSe and PMN-PT can be achieved at small scales as suggested by recent advances in materials scaling [14,15]. Early device prototypes are described in Refs. 9-10.

The need for high power-performance devices throughout the IT landscape, supports significantly extending the application space of the PET using its 4-terminal embodiment as a platform. First, sensor array monitors for structures (e.g. bridges, buildings) and human wearables, for example, are not inherently useful without computational resources to analyze and convert their output into safety and health semiotics [17]. These computational capabilities should be located on-board the sensors to avoid power hungry communication; this demands high efficiency computation in terms of Flops/Watt since only limited power resources are available to achieve both low weight and long lifetime at low cost. Here, the PET solution is a low voltage device with a high On/Off resistance ratio and moderate speed and density which we term Low Voltage - Large Area (LVLA). Second, Radio Frequency (RF) switches, devices with wide civilian and military uses such as cellphones and phased array radar have challenging specifications including power, band width and linearity, where the drive towards increased operating frequencies, and the need to reduce programming power makes new solutions attractive [18]. In the PET RF switch, the gate leads M1, M2 carry the switch control signal, while the output contacts M3, M4 carry the RF signal. Here, the key Figure of Merit is the time constant $\tau_{\mathrm{FOM}} = R_{\mathrm{On}}^{(\mathrm{PR})}C_{\mathrm{Off}}^{(\mathrm{PR})}$ which can be as low as a few femtosecond, very much lower than alternative RF switch implementations [18]. Third, we revisit the VLSI niche using the 4-terminal device platform which has the advantage of complete gate isolation allowing complementary logic with unidirectional poling of the PEs (by switching the wires), and gates such as a flip-flop SRAM not possible in CMOS [16] to be implemented.

In this letter, we optimize the 4-terminal embodiment of the PET device (Fig. 1) for three applications of interest, the VLSI scale transistor, the low voltage - large area transistor for on-board computing in sensors, and the RF switch, and describe the underlying device physics. For each device concept, the current state of fabrication techniques and materials is given. The devices are presented from small scale to large as paradoxically, the RF switch requires a more complex embodiment to achieve high performance whereas the smaller devices illustrate the basic physical concepts more cleanly.

We begin with a description of the 4-terminal PET switch and our modelling methodology. The 4-PET is a seven material layer stack, a bottom PE metal (M1), PE, top PE metal (M2), insulator, bottom PR metal (M3), PR, top PR metal (M4) and a hard surround. The void space allows for unhindered lateral motion of the PE and PR components. Optimal performance, requires high work function metals; for the PR, this choice pins the Fermi level near the valence band allowing for a maximal piezoresistive effect [19] while for the PE, this limits gate leakage [11-12]. The large areal difference between the PE and PR (as depicted in Fig. 1) serves an important purpose. As forces match at materials' interfaces and stress is force per unit area, the large area ratio, A_{PE}/A_{PR}, allows a small force generated by the PE to create a large stress in the PR - the hammer and nail effect – thereby facilitating low voltage operation. In the switch operation, the PE charges and extends to compress the PR against the hard surround when a voltage signal arrives. Since electronic time scales in the PR are of order femtoseconds, it can be assumed that the stress state of the PR determines the resistivity as the electrons can instantaneously adjust to adiabatic nuclear motion caused by PE actuation. We model PR resistivity as proportional to the negative exponential of the indirect band gap which is determined from a full deformation potentials analysis [19,20] times a gauge factor fit to experimental data [16,19-21]. The stress state in the PR material is generated from a cylindrically symmetric linear piezoelectric computation for a given voltage, V, applied across the PE [21] using ANSYS. We assume Ohmic behavior and compute the current density, and hence the current, $I(V)$, from the continuity equation; the quantity $I(V)/I(0)$ defines the On/Off ratio [21].

We next determine, for each application, the device geometry and materials choices that minimize the switching voltage, the voltage required to achieve an On/Off ratio of 10^4, with the constraint that the current density be uniform in the PR channel. The PR material is taken to be SmSe and the PE material, PMN-PT. The many device features, materials sizes and types, make statistical methods the ideal choice to develop/discover design rules and then discern the physics underlying them.

Consider the VLSI PET: the PR element is taken to be a cube of 3 nm on edge, which is sufficient to avoid the tunneling dominated transport regime [8,19]. All the other parameters in the device were sampled from uniform finite distributions (hat functions) in the philosophy of equal *a priori* probability. We took the top performers parameter sets and by graphical methods identified the important variables (See inset table to Fig 1 and Ref. [21]). The key parameters are found to be the height (thickness) and width of the PE, the total thickness of M2, INS and M3, termed H_{MIM}, and the Young's modulus of M2.

The next step is to refine the design. Figures 2a and 2b, show that the PE width should be taken approximately equal to the PE height and H_{MIM} should be taken to scale linearly with PE height; however, the thickness, H_{MIM}, is constrained to be greater than 12 nm, to allow a physically realizable individual layer thickness of $\frac{1}{3}H_{MIM} \geq 4$ nm and simply taking H_{MIM}=12 nm is shown to have little effect on performance. While all other metals in the stack optimize as elastically stiff

materials, performance improves with the introduction of an elastically compliant M2 as shown in Fig. 2c.

There are sound physics-based reasons which explain the results of our simple learning procedure; the fundamental tradeoffs in the device design are: *(i)* the PE aspect ratio (H_{PE}/W_{PE}) cannot be taken too low because the PE becomes clamped to the substrate and cannot expand sufficiently to strongly compress the PR [15]. If taken too high, the hammer-nail effect is lessened and the tall-thin structure becomes too elastically compliant, again, compromising performance. The optimal result, here, is $H_{PE}/W_{PE}\approx 1$; *(ii)* The clamping effect also occurs at the top electrode surface. Therefore, choosing a more elastically compliant M2 unclamps the PE resulting in greater extension for the same applied voltage. *(iii)* The M2/INS/M3 height, H_{MIM}, controls bending of the structure (scaling as H_{MIM}^{-3}); if H_{MIM} is taken too small, the M2/INS/M3 bows as the PE expands reducing compression of the PR, raising the voltage required to generate the desired On/Off ratio. On the other hand, if H_{MIM} is taken too large, it begins to dissipate a significant fraction of the mechanical energy generated by PE and thereby decreases the efficiency of the device. For the VLSI PET, taking H_{MIM} =12 nm works well in all cases as discussed above.

Further insight can be gleaned from a 1-dimensional compact model of the PET consisting of a PE element, a PR element, infinitely stiff and thin electrodes and insultor, and an infinitely stiff HYM, subject to an applied voltage, V [6,7]. The model provides an estimate of the uniaxial stress in the device's PR element

$$T_{33}^{(\mathrm{PR})}(V) \approx \frac{d_{33}V}{s_{33}^{(\mathrm{PR})}h + s_{33}^{(\mathrm{PE})}H_{PE}\frac{a}{A}} \quad , \qquad (1)$$

where $\{H_{PE}, W_{PE}, A=W_{\mathrm{PE}}^2\}$ are the height, width and area of the PE, $\{h,w,a=w^2\}$ are the height, width and area of the PR, d_{33} is the piezoelectric constant of the PE and $s_{33}^{(\mathrm{PR})/(\mathrm{PE})}$is the elastic compliance of the PR/PE. Assuming the resistivity scales as $\rho \approx \rho_0\exp(-\pi_u T_{33}^{(\mathrm{PR})}(V))$ [13,14,19] and taking $\{H_{PE}=W_{PE}, h=w\}$ as above, the On voltage (i.e. the voltage required to create an On/Off ratio of 10^4) is

$$V_{\mathrm{On}} \approx \left(\frac{4\ln(10)s_{33}^{(\mathrm{PR})}h}{\pi_u\, d_{33}}\right)\left(1 + \frac{s_{33}^{(\mathrm{PE})}}{s_{33}^{(\mathrm{PR})}}\frac{h}{H_{PE}}\right) \quad . \qquad (2)$$

In Fig. 2c, only $\{H_{PE}=W_{PE}\}$ is varied; hence, following Eq. (2) $V_{\mathrm{On}} \approx B(1 + C/H_{PE})$ with $\{B,C\}$ constant, a form obeyed well by the data provided renormalized PE materials properties are introduced to treat the effects of the true multi-component device structure [20]. Extrapolating the data to $H_{PE} \rightarrow \infty$, yields a lower bound for V_{On} of about 75 mV.

Based on the above results, a good choice of PE geometry for the VLSI PET is cube/pillar of edge 35 nm combined with a PR cube/pillar of 3 nm on edge as shown in Fig. 2c – a compromise between speed (the acoustic time increases linearly with PE height), line voltage, device switching energy and keeping low strain (< 1%) and stress (< 100 MPa) in the PE for stability under cycling. This device is estimated to switch at 115 mV with a clock speed of 8 GHz. The metal thicknesses are chosen such that they can be fabricated at the required scales using current methods. The PR

and PE pillars are within fundamental physical limits [8,22] but neither thin films nor patterned structures of these materials are yet available at the VLSI scale. Lithographic advances will arise from the continued CMOS Moore's Law scaling and other technologies with small features [23].

An important new application space in the IT ecosystem is on-board low electrical power/high compute power computational capability for sensor networks, to which a LVLA PET seems well-adapted. In Fig. 2c, a PE pillar of dimension 70 nm on edge is predicted to switch On at a line voltage of 95 mV. Since the PET obeys a Dennard-like scaling law [6,7,16], scaling all dimensions, the time scale and the voltage by 2x allows for a device with a 140 nm on edge PE and a 6 nm on edge PR to operate with a line voltage of 190 mV and a clock speed of 2 GHz. Scaling by 3x yields a 210 nm on edge PE pillar and a 9 nm on edge PR operating at 285 mV with a 1 GHz clock. Either of these two devices, optimized for On/Off ratios of 10^4, would result in a breakthrough in the LVLA application space if realized. We note, that high quality PE and PR films at the largest LVLA device size discussed are currently available [14,15] but fabrication into high performance pillars has yet to be demonstrated. Resistivity scaling with dimension, assumed in Dennard's scaling argument, can be achieved by varying composition of the $Sm_xEu_{1-x}S$ type PR, for example.

The stress based 4-terminal transduction device implementation of a basic RF switch is presented in Fig. 3b with 1 switch per RF line. The difference from the PET of Fig. 1 is the extension of M3 and M4 into the PR region which is referred to as the nail. This new feature is implemented to give the device the flexibility necessary to generate uniform current density in the PR [21]. In essence, the nails plus the PR form a "composite" structural element (M/PR/M) as the metal nails have the same width as the PR. The PR, itself, is selected to be of dimension 15 nm x (300 nm)^2 such the $R_{\mathrm{On}}^{(\mathrm{PR})}C_{\mathrm{Off}}^{(\mathrm{PR})}$ can be low and yet the device practicable.

We apply the statistical analysis described above to determine the key variables (see Fig. 3c) which are the same as in VLSI study with the addition of the nails which together with the PR form the new composite element. Due to the low aspect ratio of the PR itself, optimization of the PE results in a 1:1.5 height to width ratio as given in the Fig. 4a. A nail height of 100 nm is sufficient to yield a uniform current density in the PR (see Fig. 4b). Thus, a PE of dimension 900 nm x (1750 nm)^2 in conjunction with a PR of dimension 15 nm x (300 nm)^2 yields an effective RF switch with a RF Figure of Merit of $R_{\mathrm{On}}^{(\mathrm{PR})}C_{\mathrm{Off}}^{(\mathrm{PR})} \approx 4$ fs and a switching voltage < 10V (see Fig. 4c). The composite PR is nearly of dimension (300 nm)^3 - Dennard scaling of VLSI PET to this PR size would indicate a thicker PE and wider PE would be required, (3.5 μm)^3, so the composite design offers important advantages as thicker PEs are harder to process. For the optimal dimensions, both thin film materials and patterning techniques are available for the PR and the PE [14,15] and fabrication of a fully integrated RF switch is on the near horizon based on learning from our proof of concept designs [9,10]. To achieve practical application, the RF switch has to be optimized within a package [18,21] and for this work, we are developing a deep neutral net approach.

The piezoelectronic stress transduction switch has been modeled as an RF switch at the 1 μm PE scale, as a large area-low voltage logic transistor at the 140 nm PE scale, and as a CMOS replacement in VLSI at the 35 nm PE scale and physics-based design rules described. We have

shown the 4-terminal device embodiment is sufficiently flexible to deliver a RF switch with a figure of merit of 4 fs, a low voltage - large area, logic switch with a line voltage of 200 mV, 2 GHz operating frequency and a 10^4 On/Off ratio for on-board compute in sensors, and a VLSI transistor operating at 115 mV line voltage and 8 GHz operating frequency for a potential CMOS replacement. This predicted high performance across a wide range of application spaces, demonstrates that the piezoelectronic transduction device has a place in the rapidly approaching mega-data era. The results should spur the research into PR and PE scaling [14,15], and the piezoelectronic transduction switch fabrication techniques [9,10] necessary to realize the across the board, fast, low power solutions modeled here.

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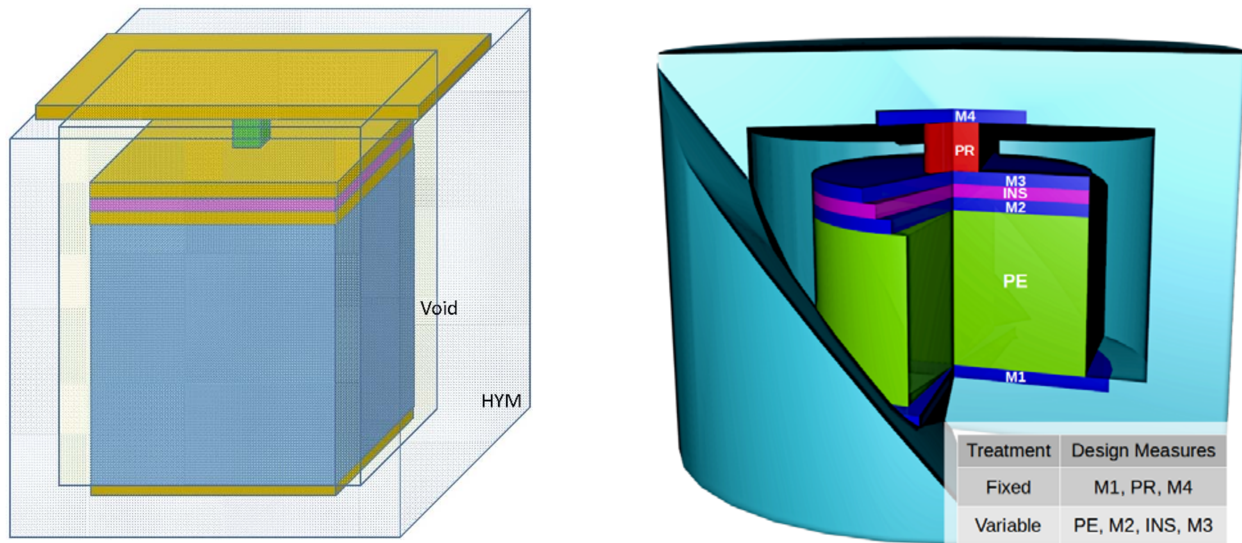

Figure 1: Left: Schematic of the 4–terminal PET for VLSI and LVLA applications – a seven material layer stack consisting of a bottom PE metal (M1), PE, top PE metal (M2), insulator, bottom PR metal (M3), PR, top PR metal (M4) and a hard surround fabricated form a high yield strength material (HYM). A void space allows free motion of the components laterally. Right: PET as modeled by ANSYS in cylindrical coordinates – rectilinear components of the 7-layer device stack are replaced by cylindrical components allowing highly efficient computations. The table in the inset gives the important design parameters: fixed indicates that the quantity is kept constant during the optimization procedure because it does not strongly effect the switching voltage while variable indicates that the quantity is exhaustively sampled in the fine-grained optimization procedure described in the text and the SI [21].

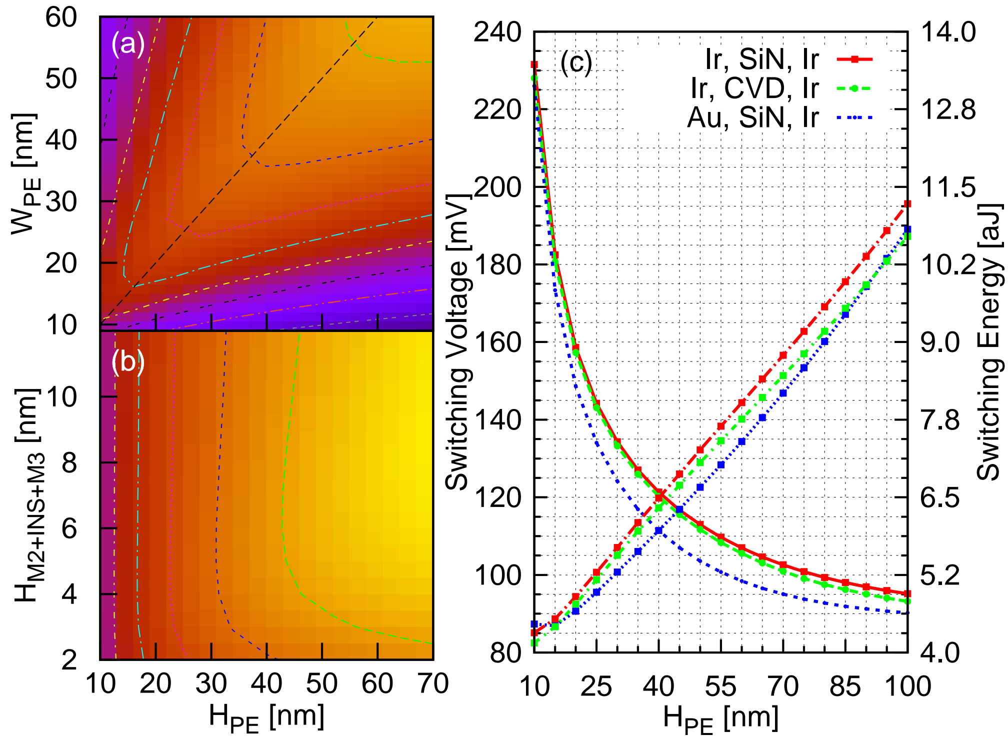

Figure 2: Panel (a) depicts the average pressure in the PR (blue: lowest, yellow: highest) as a function of PE dimension, with all other variables including applied voltage fixed. Panel (b) shows the dependence of pressure on the combined thickness of the middle layer (M2+INS+M3) with the PE fixed in a 1:1 aspect ratio. Finally, in panel (c) the switching voltage and the switching energy obtained from the continuity equation assuming Ohm's Law inside the PR (see SI [21]) is given for different material compositions of the MIM stack: (M2, INS, M3); the PR is a 3x3x3 nm^3 cuboid. We envision replacing gold by an appropriate relatively soft, high work function metallic oxide in practical applications.

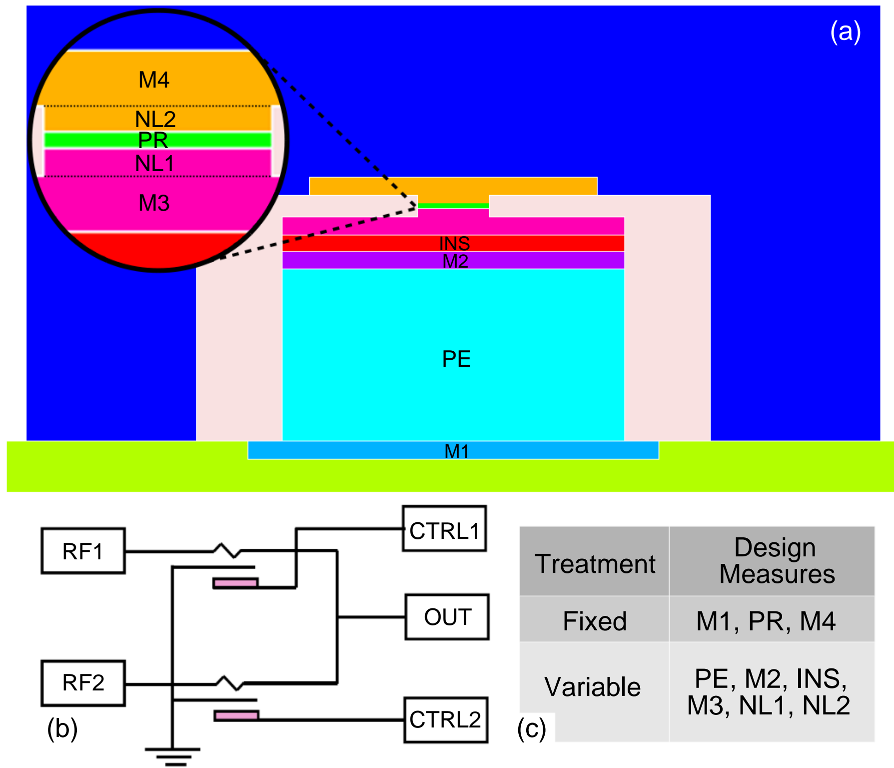

Figure 3: Panel (a) shows the schematic of a PET-based RF switch device structure made distinct from Fig. 1a by the addition of extensions to M3 and M4 referred to as nails. The scale of PR (300 nm wide) allows the nails to be fabricated using current techniques. In panel (b) the four terminal switch is implemented as an RF circuit. The switching lines are distinct from the RF signal lines for better isolation. Two RF sources are shown, each with a 4-terminal switch. In panel (c), following the same rationale as in Fig. 1, the design parameters are grouped into fixed and variable as given in the inset. The nails are necessary to reduce the non-uniformity of the stress distribution in the PR and hence the current density.

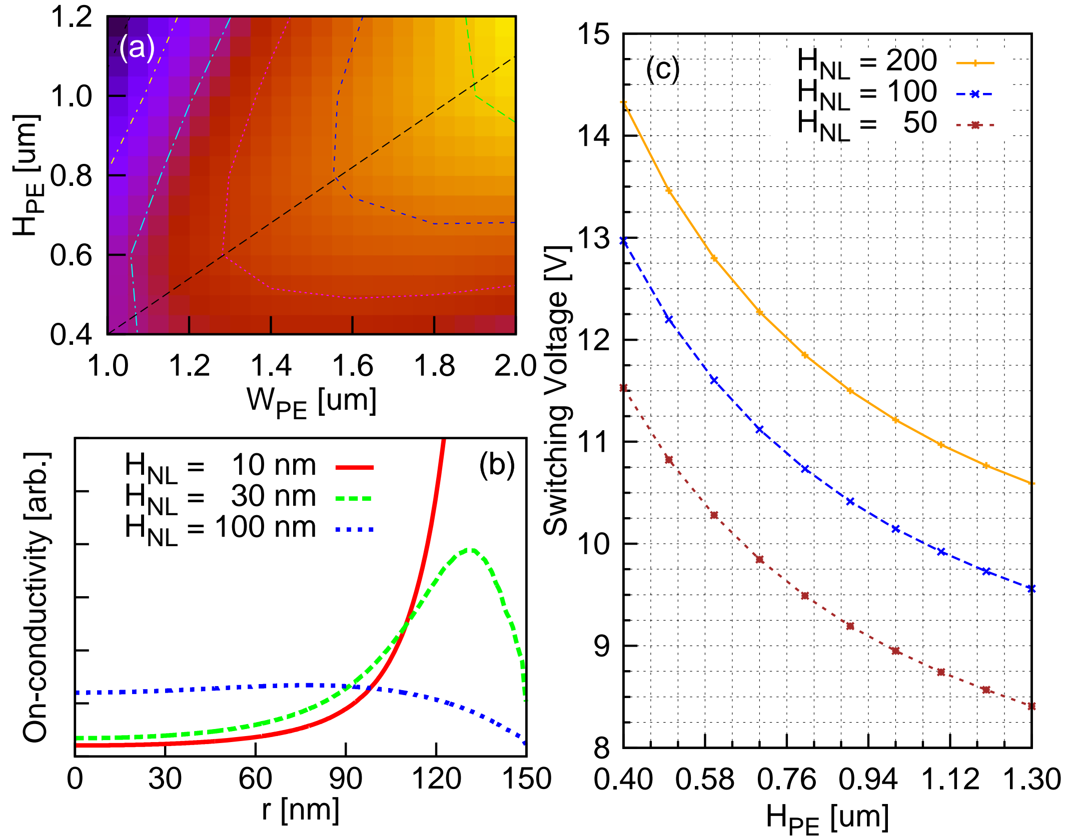

Figure 4: Panel (a) shows the pressure in the PR as a function of the dimensions of the PE with all other design parameters fixed. Panel (b) illustrates the conductivity radially across the PR at mid height for different nail heights. In panel (c), the required switching voltage of the RF switch at different PE scales is presented (with the PE fixed in the optimal aspect ratio described in panel (a)) for several nail heights. The switching voltage was computed by solving the continuity equation assuming Ohm's Law is valid inside the PR and then used to estimate the switching energy (see SI [21] for details).