A TCAD and Spectroscopy Study of Dark Count Mechanisms in Single-Photon Avalanche Diodes

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Eric A. G. Webster, *Member, IEEE*, and Robert K. Henderson, *Member, IEEE*

***Abstract*— It is shown through dark count rate spectroscopy (DCRS) and TCAD-simulations that in single-photon avalanche diodes (SPADs), the majority of low dark count rate (DCR) devices in modern CMOS arrays are free of deep-level traps and that DCR can therefore be explained by saturation current and band-to-band tunneling (BTBT). The DCRS performed on the Megaframe 32 x 32 show that the activation energies for the high DCR devices are consistent with a single type of defect at ≈0.44 eV, thought to be the E-center, in differing electric fields. Calibrated TCAD-simulated reverse bias leakage currents are orders of magnitude lower than those measured due to the lack of parasitic leakage paths but give theoretical DCRS that are close to the measured values for four different SPAD designs and predict the voltage dependence at high fields. The coefficients for Kane's indirect tunneling model in the [100] direction are determined as $A \approx 2 \times 10^{15}$ cm^{-3}/s and $B \approx 2.39 \times 10^{7}$ V/cm through TCAD calibration, DCR measurement, and theory. It is found that indirect BTBT dominates the DCR of SPADs with low breakdown voltages.**

***Index Terms*— Avalanche diodes, dark count rate (DCR), dark current spectroscopy, noise, single-photon avalanche diode (SPAD), TCAD, tunneling.**

I. Introduction

THE dark count rate (DCR) of single-photon avalanche diodes (SPADs) is the parasitic count rate attributed to natural carrier generation processes inside the diode, well understood to be Shockley–Read–Hall (SRH) [1], [2] trap-assisted generation, thermal generation, and diffusion saturation currents [3]–[6]. In SPADs, another major contributor to the leakage current is band-to-band tunneling (BTBT) [7] because of the high reverse bias and narrow junctions. The SPADs that are tunneling-dominated have very high DCRs of the order of hundreds of kilohertz [8], [9]. Indeed, BTBT is the dominant factor that contributes to the trend of higher DCR with process node shrink apparent from the literature. Additionally, the combination of traps and high electric field leads to trap-assisted tunneling and Poole–Frenkel barrier force lowering, further increasing the DCR [5], [6], and [10].

It is possible to create SPADs with low DCR by avoiding the onset of tunneling in custom processes [11]–[13] and recently DCRs approaching tens of hertz [5], [11], [14]–[16] at room temperature have been reported in CMOS SPADs. Interestingly, SPADs typically have a DCR distribution where a small proportion of devices have very high DCR [11], [17]–[19].

Modern SPADs in CMOS and custom processes are enabling many new applications for solid-state single-photon counting and timing such as time correlated single-photon counting in fluorescence lifetime applications [20], 3-D-imaging and ranging [21], and positron emission tomography [11]. There is therefore an increased interest in methods of predicting SPAD DCR prior to fabrication to accelerate technology development, rather than relying on iterative design. Modeling the DCR of SPADs has been a topic of study since they were first developed in the early 1960s [22]. Recent approaches to DCR modeling generally assume the presence of deep-level traps to fit the measured results [23]–[25].

This paper describes a different approach to DCR modeling to previous efforts, which are reviewed first. Dark count rate spectroscopy (DCRS) results are then presented, which suggest that only a small proportion of devices are influenced by traps in different local electric fields and have high associated DCR; whereas the rest are trap-less. It is therefore proposed that calibrated TCAD simulations can be used to predict the DCR of trap-less SPADs. To support this, the calibration of the TCAD simulated to measured breakdown voltages is then presented using STMicroelectronics confidential information. Trap-less SPADs are considered as ideal devices for studying BTBT and therefore the BTBT model in TCAD is calibrated on three different multiplication junctions. Finally, the results are discussed and conclusions are given.

II. Previous Approaches to DCR Modeling

Assuming that the same mechanisms are responsible for reverse bias leakage current and dark counts, previous researchers have tried to match the measured DCR with the measured current divided by the electronic charge, q. However, this resulted in DCRs many orders of magnitude higher than measured. For example, for the SPAD reported in [14] with DCR ≈40 Hz at room temperature, the 8.95×10^{-10}A leakage current at breakdown predicts ≈5.5 GHz. Pagano *et al.* [25] assumed a high trap concentration and associated high generation current to match the leakage current of an array of SPADs. However, the small leakage current of micrometer-scale SPADs is easily overestimated due to imperfectly sealed RF environments, measurement equipment limitations; and parasitic leakage paths in the test equipment wiring, PCBs, and CMOS dielectric stack, as well

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as in the SPAD through the guard ring and due to surface generation, all of which is not multiplied and therefore does not contribute to dark count.

Kang *et al.* [23] take an alternative detailed probabilistic approach to DCR modeling. This method also assumes the presence of traps with high concentration to match the measured primary dark current to the DCR. However, the presence of high trap concentrations is likely in the III–V devices discussed. Such high trap concentrations are unlikely for modern CMOS SPADs and associated high quality processing. Similarly, Kindt and van Zeij1 [24] assume the trap-assisted tunneling DCR model, and associated parameters, and do not discuss the varying DCRs of different devices.

III. Dark Count Rate Spectroscopy

Many authors report DCR distributions where a fraction (5% to 20% or higher, depending on process and device size) of SPADs have a very high DCR [6], [11], [16]–[19]. It is proposed that it is this small proportion of devices that have traps.

DCRS was thought to be a good method of testing this hypothesis. DCRS builds on the dark current spectroscopy that was developed by McGrath *et al.* [27] for studying deep-level traps in CCDs. The development of large CMOS SPAD arrays has made it practical to apply the per-pixel DCS technique to obtain a large sample size [28].

To perform the experiment, a Megaframe 32 × 32 [28] sensor of the same batch as presented in [19] with ≈80% low and ≈20% high DCR devices was placed in a temperature controlled oven. The temperature was increased in 5-K increments from 293 to 343 K and ten 1-s integrations for each pixel captured and averaged at each temperature. The activation energy (E_A) of each of the 1024 SPADs was then calculated using the Arrhenius equation. A histogram of the resulting activation energies is illustrated in Fig. 1. The Meyer–Neldel relationship (MNR) [29] was also observed between E_A and preexponential factor and was corrected for in the same manner as in [29]. The total capture cross section, σ_t, was calculated using the same technique as [29], with the volume calculated from the layout and TCAD-simulated junction width and the results shown in Fig. 2.

Fig. 1 shows that there are two distributions of E_A, one at ≈0.85 eV and ≈0.45 eV. The 0.85-eV peak corresponds to the 80% low DCR devices and is consistent with normal diode generation and diffusion leakage current. The 20% of devices with high DCR have $E_A \approx 0.45$ eV. However, from Fig. 2, it is clear that this corresponds to a wide spread in effective σ_t. This is consistent with the trap existing in different electric fields as can be seen from the general trend of larger σ_t with smaller E_A. This is thought to be a manifestation of the Poole–Frenkel barrier force lowering and trap-assisted tunneling.

It is likely that the ≈0.45-eV level corresponds to the E-centre (phosphorus-vacancy) defect given the agreement with prior DCS work [29]. In addition, in the case of these devices [15] manufactured in a CMOS imaging process, it is known that there is negligible contamination. This is unsurprising given that CMOS image sensors require low dark currents

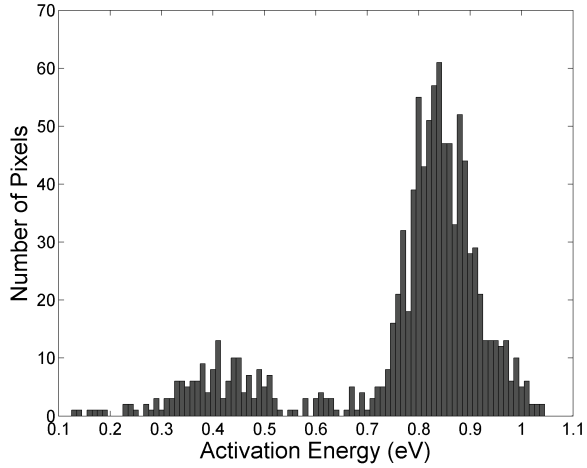

Fig. 1. Histogram of measured activation energies.

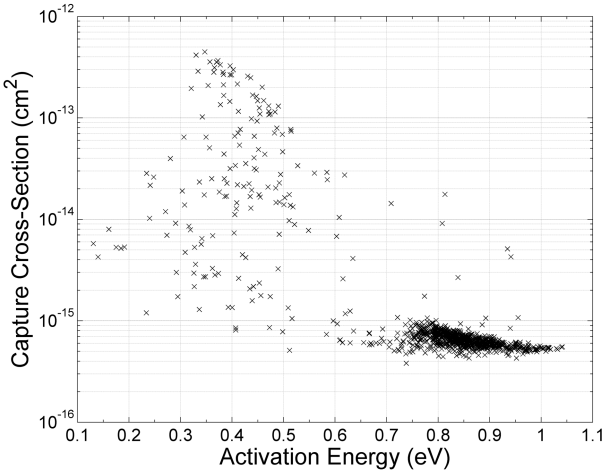

Fig. 2. Scatter plot of measured E_A against calculated σ_t using MNR correction.

for high signal-to-noise ratios in low light conditions. This might not be the case for SPADs manufactured in high voltage or digital CMOS technology, however.

The higher relative probability of having a high DCR SPAD pixel of ≈20% compared with a high dark current pixel of ≪1% in CMOS image sensors can be attributed to the larger 6-μm diameter active area of SPADs in [28] relative to 1.75-μm pitch pixels [29]. From the presented results, it is thought that the DCR variation among the ≈20% high DCR devices is accounted for by E-centers in different electric fields.

If, therefore, it is only the high DCR devices that are influenced by traps, a different mechanism is required to explain the DCR of trap-less devices. The focus of the rest of this paper is on predicting the median DCR of trap-less SPADs of differing designs. It is proposed that this can be predicted with commercial TCAD simulation tools.

IV. TCAD Simulation Methods and Calibration

A. TCAD Process and Device Simulation Methods

Simulations were performed with the Synopsys Sentaurus TCAD suite using STMicroelectronics' proprietary process

calibration data [30]–[32]. The front-end flow was simulated with Monte Carlo (MC) implants.

The 2-D process and electrical simulations were performed of 1-μm^2 SPAD multiplication junction and appropriate depth with reflective boundary conditions at the noncontact sides to eliminate any guard ring effects. The simulated current could then be scaled to the dimensions of real devices. The small simulation domain reduced the MC implant and electrical simulation run times. A tensor mesh was chosen for simplicity with adaptive refinement on the doping concentration gradient to resolve the high electric fields.

Stratton's hydrodynamic electron transport model [33] was chosen to describe the high field narrow junctions present in advanced CMOS processes. Avalanche generation and Auger recombination heat sources/sinks were accounted for [34]. The Philips unified mobility model was used with the donor species of the junction specified [35]. Velocity saturation was included with the Canali [36] model. Avalanche multiplication was modeled according to van Overstraeten [37] with Auger recombination [32] included because it is the inverse process [4]. The SRH generation/recombination was disabled for consistency with the zero-trap hypothesis.

Apparent band gap narrowing (BGN) at high doping concentrations influences the effective intrinsic carrier concentration [38] and therefore the saturation current. The different BGN models available in TCAD were found to influence the saturation current by a factor of $\approx$4 for the devices studied. The BGN was therefore modeled according to del Alamo [38] that gave BGN in the middle of the range. It is not clear which BGN model is the most reliable; and therefore, BGN is a source of uncertainty in this paper.

The BTBT was simulated with the dynamic nonlocal model [7], [32]. Hurkx [39], [40] reported the TCAD default A and B parameters as $A = 4 \times 10^{14}$ cm^{-3}/s and the critical field $B = 1.9 \times 10^7$ V/cm. There have been several attempts to determine the coefficients and critical field for BTBT in silicon [39]–[41] and values of B range from 1.9×10^7 [40] to 3.1×10^7 V/cm with a theoretical value of 2.2×10^7 V/cm reported in [41]. Importantly, for large area devices in old processes the absence of traps, and therefore trap-assisted tunneling, which would dominate the leakage, could not be excluded. It is therefore likely that prior work over-estimated BTBT.

SPADs allow measurement of the ideal BTBT rate that is not possible with other devices for two reasons: 1) only current flow across the multiplication junction contributes to the DCR, which is simply measured macroscopically with a pulse counter and 2) SPADs can be considered trap-less if they are not from the high DCR tail (Section III).

For the CMOS SPADs studied, tunneling occurs in the [001] direction for electrons from the light hole band to the transverse conduction band. Therefore, $m_e = 0.19m_0$ and $m_h = 0.16m_0$ [4] was assumed for the calculation of B in the Kane model [7], [32], where m_0 is the rest electron mass. Assuming zero conduction band offset, this gave $B \approx 2.39 \times 10^7$ V/cm, which is near identical to [42] and is within the theoretical range of [41], whereas higher than that determined by Hurkx. The A was used for fitting because calculation from theory requires knowledge of D_p, the phonon deformation potential, for which there are many different values [43].

TABLE I
SIMULATED AND MEASURED BREAKDOWN VOLTAGES

SPAD Multiplication Junction	Measured V_{BD} (V)	Simulated V_{BD} (V)	Error (V)
p-well/DNW [15]	13.95	13.72	−0.23
$p-$/DNW [15]	18.00	18.15	+0.15
DNW/$p+$ substrate[44]	14.90	14.81	−0.09
DNW/$p-$ substrate [45]	20.00	20.05	+0.05

B. Breakdown Voltage Calibration

TCAD calibration was performed on the breakdown voltage (V_{BD}). Measurements were performed with an HP4156B parameter analyzer. Model validation was complicated by the fact that the breakdown voltage varies part-to-part and so it was attempted to find a match to the typical breakdown voltage. Table I lists that measurement and simulation are in good agreement for two devices reported in [15]: 1) the p-well and p$^-$ designs and 2) the deep n-well (DNW)/p-substrate design with a high [44] and low substrate doping [45].

V. DCR MODELING

A. Methods

Sentaurus TCAD interestingly allows simulation of the nonphysical reverse I–V characteristic without avalanche generation enabling observation of the leakage current above breakdown. This is physically valid for SPADs because impact ionization multiplies the current when primary carriers are generated. There is no avalanche multiplication if there is no primary carrier and the generation rate should be the same above or below the breakdown voltage, except for increased generation at higher bias due to tunneling.

Interestingly, the simulated saturation current was six to eight orders of magnitude less than measured because of the lack of parasitic leakage. Given the ultralow saturation current simulation results, it is worth evaluating whether TCAD can simulate the trap-less DCR of different device designs.

To evaluate this in detail, three device designs were studied: DNW/p-substrate designs of different substrate concentration and therefore breakdown voltage [44], [45] for which good DCR versus voltage data was available; and the p-well device of [15] for which there was a large sample size, but the voltage range was limited due to the transistor gate oxide.

B. Results

The simulated SPAD leakage current with different values of A, expressed in electrons/s for comparison to the measured DCR (hertz), is shown in Figs. 3–5 for the DNW to p-substrate junction with a lightly [45] and heavily doped substrate [44], and the p-well device of [15], respectively. Table II lists the results and shows the simulated and measured DCR at $V_{BD} + 1$ V (A) without (I_{SAT}) and with (I_R) tunneling using $A = 2 \times 10^{15}$ cm^{-3}/s and $B = 2.39 \times 10^7$ V/cm.

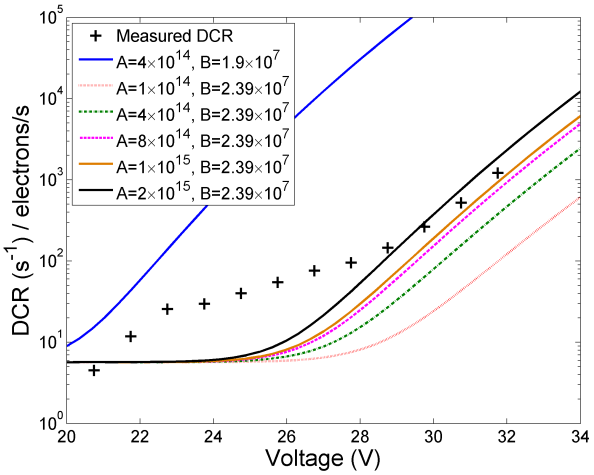

Fig. 3. DNW/p^- substrate SPAD tunnelling calibration [40].

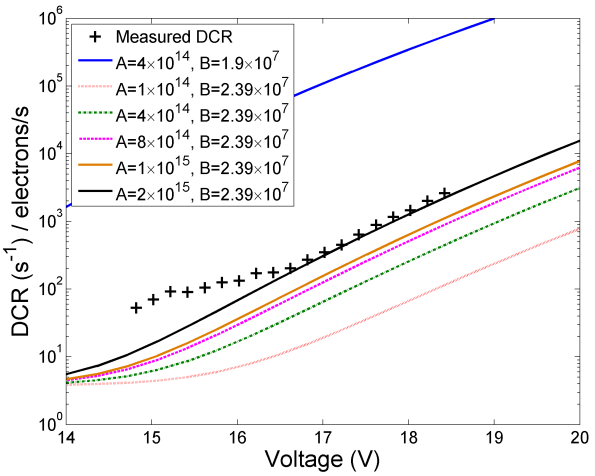

Fig. 4. DNW/p^+ substrate SPAD tunnelling calibration [39].

The results show that in all cases the Hurkx parameters vastly over-estimate the DCR. Better agreement is achieved with the theoretically determined critical field. However, the results do not match at low bias levels for the DNW/substrate devices but is in reasonable agreement for the p-well device.

For >16.5 V with the highly doped substrate [44] and >28 V with the lightly doped substrate [45], there is an agreement between the simulated and measured DCRs with $A = 2 \times 10^{15}$ cm^{-3}/s, close to the theoretical value of 3.29×10^{15} cm^{-3}/s in [42] at biases where the activation energy decreases to $< E_g/2$ [44], [45]. The deviation from tunneling-dominated leakage below this voltage could be attributed an increased saturation current relative to that simulated due to possible minority carrier effects (Section VI) [46]. A changing avalanche breakdown probability (ABP) could account for the different DCR vsersus voltage gradient in this region. The ABP is expected to be close to one at high bias [45].

The results do not agree for the p-well device [15] with $A = 2 \times 10^{15}$ cm^{-3}/s. The simulations predict tunneling-dominated DCR ≈600 Hz at 1 V excess bias when the measured DCR is known to be ≈50 Hz and dominated by

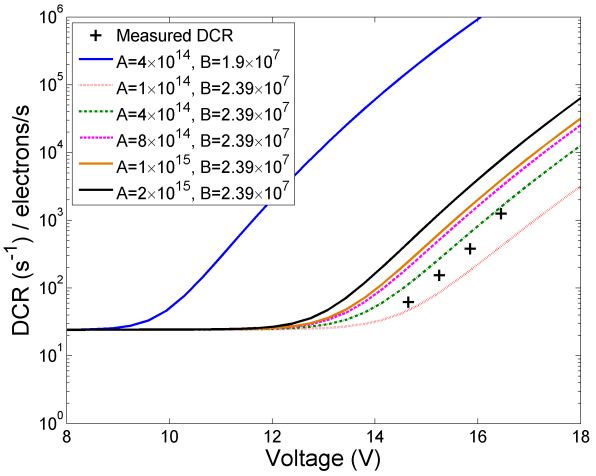

Fig. 5. p-well/DNW SPAD tunnelling calibration [15].

TABLE II
SIMULATED AND MEASURED DCR

SPAD Multiplication Junction	Simulated I_{SAT} [no tunneling] (electrons/s)	Simulated I_R [with tunneling] (electrons/s)	Measured DCR of trap-less devices (Hz)
p-well/DNW [15]	≈26	≈600	≈50
$p-$/DNW [15]	≈30	≈30	≈50
DNW/$p+$ substrate[44]	≈4	≈4	≈100
DNW/$p-$ substrate [45]	≈6	≈6	≈18

thermal generation (Section III). This could be because of the slight under-estimation of V_{BD}. As V_{BD} reduces, the field increases and therefore a small error in V_{BD} means a large error in field that corresponds to an exponential tunneling error. An increase in simulated V_{BD} by 0.23 V (Table I) would shift the simulated tunneling current to the right in Fig. 5 giving better agreement with $A = 2 \times 10^{15}$ cm^{-3}/s. Interestingly, the simulated saturation current appears to agree well with measurement.

VI. DISCUSSION

Overall, the simulations give reasonable agreement with measurement without making the widespread trap assumption. The main discrepancy is the lack of agreement between the saturation current and DCR in both substrate-based SPAD designs with rough agreement for the p-well device.

The disagreement in saturation current is possibly explained by nonequilibrium minority carrier effects, which TCAD does not simulate at equilibrium. Transient TCAD simulations show that during breakdown electrons and holes diffuse opposite to the direction of electric field, i.e., electrons from n-type diffuse into p-type and vice versa [46]. This would lead to a new steady-state minority carrier density in the vicinity of the junction being established leading to increased saturation current and therefore DCR. For the p-well device, this is not such a problem due to the collector action of the DNW/substrate junction [46]. Minority carrier effects are therefore a possible avenue of future investigation. An alternative is that the guard

ring contributes to the DCR. However, the close agreement obtained with the p-well device's saturation current and DCR suggests this is not the case. Additionally, BGN influences the saturation current and in general appears uncertain in the literature.

The tunneling is fitted well with $B = 2.39 \times 10^7$ V/cm and $A = 2 \times 10^{15}$ cm^{-3}/s for the SPADs where there is the highest confidence in the accuracy of the TCAD simulated field [44], [45]. However, from the measurement results on all devices A varies over the range $1 \times 10^{14} - 2 \times 10^{15}$ cm^{-3}/s while $A = 2 \times 10^{15}$ cm^{-3}/s corresponds closely to 3.29×10^{15} cm^{-3}/s theoretically calculated by Kao [42]. However, there is significant uncertainty regarding D_p for each phonon mode [43] and it has been observed that both the transverse optical (TO) and transverse acoustic (TA) phonons contribute equally [41].

All phonon modes are thought to contribute to indirect tunneling and therefore A determined from fitting experimental results corresponds to this combination. To illustrate the importance of the chosen values in the calculation of A and B, using the deformation potentials and phonon energies determined in [43] for the TO, TA, and longitudinal optical and acoustic phonons (LO/LA), and using values of the other coefficients from [42], gives $A_{\mathrm{TA}} = 1.34 \times 10^{14}$ cm^{-3}/s, $A_{\mathrm{TO}} = 3.53 \times 10^{14}$ cm^{-3}/s and $A_{\mathrm{LO/LA}} = 1.14 \times 10^{15}$ cm^{-3}/s. These combine to give $A = 1.63 \times 10^{15}$ cm^{-3}/s, in fair agreement with measurement. This result agrees with the observation of Logan and Chynoweth [41] that the contribution of TA and TO phonons is roughly equivalent while suggesting strong importance of LA/LO phonons that was not found [41]. For TO and TA phonons combined to equal 2×10^{15} cm^{-3}/s, then D_{TA} and D_{TO} are calculated as $\approx 1.4 \times 10^8$ and $\approx 2.6 \times 10^8$ eV/cm, respectively, from [32], which is within the known range [43]. This suggests that the method proposed for studying BTBT and the TCAD nonlocal model is valid.

VII. Conclusion

The DCRS results presented show that it is only the high DCR SPADs that are influenced by a deep-level trap, tentatively identified as the E-center in the Megaframe sensor. Therefore, through process modification, it should be possible to remove these defects to improve SPAD yield. The DCR obtained from the trap-less TCAD-simulated saturation currents is in close agreement with the measured DCR. Combined with the DCRS results, it can be concluded that DCR is not always due to traps. It is thought that doping variation could explain variability in the low DCR devices. Additionally, the TCAD simulations show that low DCR can be achieved by avoiding the onset of BTBT. This is simply obtained by designing the breakdown voltage to be $\sim$20 V that gives a $>$5 V excess bias margin to tunneling-dominated DCR at room temperature. It is therefore clear that valid DCR performance comparison can only be made between SPADs with approximately the same V_{BD}. Indeed, the typical p$^+$/n-well junction used to form SPADs is more lightly doped at larger process nodes leading to lower DCR.

It is also interesting that SPADs appear ideal for studying BTBT because single electron generation can be measured by macroscopic pulse counting. The results suggest that prior models over-estimated the tunneling rate as a result of parasitic leakage and the likely presence of traps, both of which are excluded in this paper. The measured data is fit quite well with a critical field of $B = 2.39 \times 10^7$ V/cm and $A = 2 \times 10^{15}$ cm^{-3}/s. Further calibration is required to account for nonequilibrium minority carrier effects that can be expected to influence the DCR as well as provide a trap-less after pulsing mechanism required to explain the after pulsing observed on all devices [14], [44]–[46].

Although TCAD may not yet yield the exact DCR for a given device, it is certainly possible to compare different multiplication junction design proposals for expected noise prior to manufacture, which was not possible before. The demonstrated usefulness of DCRS to study traps offers potential to guide process development to maximize SPAD yield.

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