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High-Level Hardware Feature Extraction for GPU Performance Prediction of Stencils

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Abstract

High-level functional programming abstractions have started to show promising results for HPC (High-Performance Computing). Approaches such as Lift, Futhark or Delite have shown that it is possible to have both, high-level abstractions and performance, even for HPC workloads such as stencils. In addition, these high-level functional abstractions can also be used to represent programs and their optimized variants, within the compiler itself. However, such high-level approaches rely heavily on the compiler to optimize programs which is notoriously hard when targeting GPUs.

Compilers either use hand-crafted heuristics to direct the optimizations or iterative compilation to search the optimization space. The first approach has fast compile times, however, it is not performance-portable across different devices and requires a lot of human effort to build the heuristics. Iterative compilation, on the other hand, has the ability to search the optimization space automatically and adapts to different devices. However, this process is often very time-consuming as thousands of variants have to be evaluated. Performance models based on statistical techniques have been proposed to speedup the optimization space exploration. However, they rely on low-level hardware features, in the form of performance counters or low-level static code features.

Using the Lift framework, this paper demonstrates how low-level, GPU-specific features can be extractable directly from a high-level functional representation. The Lift IR (Intermediate Representation) is in fact a very suitable choice since all optimization choices are exposed at the IR level. This paper shows how to extract low-level features such as number of unique cache lines accessed per warp, which is crucial for building accurate GPU performance models. Using this approach, we are able to speedup the exploration of the space by a factor 2000x on an AMD GPU and 450x on Nvidia on average across many stencil applications.

1 Introduction

Recent years have witnessed the emergence of high-level approaches for high-performance computing such as Accelerate [22], Futhark [10], Delite [4], Lift [35] and AnyDSL [19]. They enable programmers to write hardware-agnostic code while putting the burden on the compiler to extract performance. Tuning a compiler is very laborious and time-consuming, especially when considering accelerators such as GPUs (Graphics Processing Units) and this process has to be repeated for every new hardware generation.

Lift proposes to use rewriting [34] to solve this problem.Rewriting for compiler optimizations is an approach first proposed in 2001 in the Haskell compiler [30]. Lift’s rewrite rules attempt to define the set of all possible algorithmic and, crucially, hardware-specific optimizations. Rewrite rules liberate compiler writers from having to implement hard-coded optimizations and make it easy to extend the compiler. Optimizations are simply implemented as rules and a generic rewriting engine explores the space automatically.

However, this approach results in a large optimization space. The optimization process takes a few hours for stencils on GPUs [9], even when using an efficient auto-tuner [1]. In response, this paper develops an automatic performance model predicting the best optimized program variant using static features from the high-level Lift IR. This removes the necessity for compiling and running programs which accounts for the majority of the exploration time.

The use of performance modeling for GPUs is not novel [11, 12, 26, 27, 38]. However, to the best of our knowledge, this is the first paper to show how information about low-level GPU-specific features is extractable from a high-level functional IR. This paper demonstrates that a high-level IR is amenable to the extraction of low-level information useful for predicting performance using high-level semantic information. It also shows how cache locality information is extractable at this level. This relies on the use of the rich information stored in the Lift type system together with the ability to reason about array indices in a symbolic manner.

Using the extracted features, a performance predictor is built using machine-learning. This leads to a highly accurate model for the stencil domain, an important class of high-performance code. The model achieves a correlation of 0.8 and 0.9 on GPUs from Nvidia and AMD, respectively. Using the model to search the space requires less than 5 runs in the majority of the cases to achieve performance within 90% of the best available. In comparison, a random search requires 100s of runs in the majority of the cases.

To summarize, the paper makes three contributions:
This process is time consuming as it produces a large number of kernels (1,000 for this paper). In addition, every LIFT generated kernel is executable with a different number of threads leading up to 10,000 kernel executions.

**Time breakdown** Figure 2 shows the percentages of the time spent in the different stages of the current LIFT compilation and exploration. Unsurprisingly, the last part of LIFT’s workflow, the kernel execution, requires by far the most time (up to 90%). For this paper, executing all kernels for a single application, including the exploration of thread configurations took up to 41 minutes while all kernels were generated in less than a minute, which is about 2% of the overall time.

**Using a Performance Predictor for Exploration** The major bottleneck for exploration is clearly the OpenCL compilation and execution time of the generated kernels, which represent 98% of total time. This paper addresses this bottleneck by using a trained performance predictor directly on the transformed LIFT expression. Figure 1b shows how the exploration strategy is modified with a performance model.

Once the transformed expressions have been produced, the idea is to extract features that are informative about performance. These features are fed into a predictive model which almost instantaneously ranks the transformed expressions. Then, the transformed expression with the fastest predicted performance is selected, the corresponding kernel generated, compiled and finally executed.

While this approach seems very simple, the challenges are two-fold. First, we need to identify features that are informative about performance, such as memory access patterns. Then, they need to be extracted from the high-level functional LIFT IR. As we will see, the LIFT IR encodes all the required information to calculate low-level GPU-specific features. The next section gives background information about the LIFT IR while Section 4 will discuss feature extraction.

3 Background
This section introduces OpenCL, the existing LIFT IR, and the rewrite systems used to produce efficient OpenCL kernels.

3.1 OpenCL
An OpenCL program (kernel) is executed by multiple threads (work-items) organized in work-groups, providing a two-level thread hierarchy. Both work-items and work-groups are organized in three-dimensional grids identified by unique IDs. On GPUs, multiple
work-groups are executable on a core, and work-items are scheduled in groups of 32 for Nvidia (warp) or 64 for AMD (wavefront). It is generally desirable to start a large thread number to reach maximum occupancy.

OpenCL provides a three-level memory hierarchy: Global memory is accessible by all work-items and throughput is maximized when threads in the same warp/wavefront access the same cache line (coalesced accesses). Work-items of the same group communicate via a fast shared local memory, and each work-item has its own private memory.

3.2 Lift IR
Lift [34, 35] is a functional language based on lambda calculus, offering a small set of reusable primitives. It is a compiler-internal data-parallel intermediate language and is compiled to high-performance OpenCL code. Lift’s distinguishes algorithmic primitives which express what to compute, from OpenCL-specific primitives which express how to compute by explicitly mapping computations to the OpenCL programming model. Lift’s type system supports scalar types (e.g. int, float), tuple-types (denoted as U × T), and array-types (denoted as [T]n), where the array size n is part of the type.

Algorithmic Primitives Lift provides well-known functional primitives defined on arrays as listed below:

- **map**: (f : T → U, in : [T]n) → [U]n
- **reduce**: (init : U, f : (U, T) → U, in : [T]n) → [U]1
- **zip**: (init1 : [T]n, init2 : [U]n) → [T × U]n
- **iterate**: (init : [T]n, f : [T]n → [T]n, m : int) → [T]n
- **split**: (m : int, in : [T]n) → ([T]m) × ([T]n−m)
- **join**: (in : [[T]m]n) → [T]m×n
- **slide**: (size : int, step : int, in : [T]n) → [T]size
- **pad**: (i : int, r : int, h : (i : int, len : int) → int, in : [T]n) → [T]n+r
- **at**: (i : Cst, in : [T]n) → T
- **get**: (i : Cst, in : T1 × T2 × ... → T1
- **array**: (n : int, f : (i : int, n : int) → T) → [T]n
- **userFun**: (s1 : ScalarT, s2 : ScalarT′, ... → ScalarU

Lift supports the definition of arbitrary scalar-based sequential OpenCL-C functions called userFun. These are directly embedded in the generated OpenCL code.

OpenCL-specific primitives Lift’s OpenCL specific primitives expose OpenCL’s thread and memory hierarchy. These primitives are used to explicitly dictate how to perform the computation expressed with the algorithmic primitives.

Parallelism is exposed via specialized variations of map: mapGlobalD, mapWorkgroupD, mapLocalD, and mapSeq. These primitives directly correspond to OpenCL’s thread hierarchy. The computation specified within a OpenCL-specific map is performed by its particular level and dimension d ∈ {0, 1, 2} of the thread hierarchy, or executed sequentially by a single thread (mapSeq). OpenCL’s memory hierarchy is exposed via toGlobal(f), toLocal(f) and toPrivate(f), which specify where the output of the function f is stored in memory.

3.3 Rewriting
Lift encodes optimizations as semantics-preserving rewrite rules. These rules are used to transform a high-level expression written using the algorithmic primitives into a transformed expression in which parallelism and memory is explicitly exploited. Similar to Lift’s primitives, rewrite rules are also categorized into algorithmic or OpenCL-specific rules. Algorithmic rules such as the divide-and-conquer rule:

map(f) → join ◦ map(map(f)) ◦ split(n)

create a space of possible algorithmic implementations for the same expression. OpenCL-specific rules such as:

map(f) → mapGlobalU(f)

map expressions to the OpenCL’s programming model.

3.4 Example
Listing 1 shows a 1D 3-point stencil expressed in Lift [9]. pad is applied adding one element (0) to the left and right of the input array arg to implement a simple boundary handling. slide creates overlapping neighborhoods of three elements which are summed up using map and reduce.

Applying rewrite rules leads to Listing 2, where overlapped tiling has been applied. Every tile is processed by a work-group (mapWrg) loading all elements to local memory and computing the output using its work-items before storing it in global memory. From this expression high-performance OpenCL code is generated as shown in [9].

4 Feature Extraction
This paper proposes a performance model that predicts the performance of transformed Lift expressions on GPUs in order to identify the best variant. The model relies on static features extracted from the high-level Lift IR. Although the features are extracted at a high-level, they capture information about low-level hardware features. They broadly fall into three categories as seen in Table 1.

4.1 Parallelism
For a fixed input size, the number of launched threads influences how much parallelism versus sequential work is performed. We include both global and local thread counts across the three thread dimensions as features. Local thread count affects how large each work-group will be, which may affect data reuse or the number of concurrent groups.
4.2 Memory

This section covers the features related to the amount of memory allocated, number of accesses, and access patterns.

4.2.1 Local memory usage

One of the important factors that determines performance on a GPU is occupancy. Occupancy is typically maximized when multiple work-group execute concurrently. More concurrent work-groups typically translates to more threads executing concurrently, which ultimately helps hiding memory latency.

The number of work-groups that execute simultaneously on a core depends on the amount of resources used by each work-group. One important resource is the amount of fast local memory (shared memory) used by the work-group. Therefore, it is crucial to determine this quantity.

Extracting the amount of local memory used in a LIFT program is straightforward. The program is traversed once, collecting memory allocation sizes and summing up these numbers.

4.2.2 Number of Memory Accesses

Performance is largely affected by the amount and type of memory operations. Applications that exhibit large amount of data re-use will benefit from exploiting the fast local memory. The program can simply reuse the data in local memory several times, reducing the number of global memory accesses, resulting in increased performance.

Algorithm The LIFT code generator only produces loads and stores to memory when a user function is called. Therefore, counting the number of loads and stores boils down to counting how often each user function is called. As can be seen in Algorithm 1, a depth-first traversal is performed on the IR while keeping track of the number of times the body of patterns generating loops is executed. Once a user-function is reached, the feature extractor simply updates the total number of loads and stores. In addition to this, the extractor keeps track of the type of memory being accessed, local or global, using the toLocal and toGlobal patterns. The information about the address space is encoded directly into the IR and is populated by another pass that runs prior to feature extraction. The number of global/local loads and stores is then normalized by the number of total threads.

**Table 1.** List of extracted features

<table>
<thead>
<tr>
<th>Type</th>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallelism</td>
<td>global size (dimensions 0, 1 and 2)</td>
</tr>
<tr>
<td></td>
<td>local size (dimensions 0, 1 and 2)</td>
</tr>
<tr>
<td>Memory</td>
<td>amount of local memory allocated</td>
</tr>
<tr>
<td></td>
<td>global stores per thread</td>
</tr>
<tr>
<td></td>
<td>global loads per thread</td>
</tr>
<tr>
<td></td>
<td>local stores per thread</td>
</tr>
<tr>
<td></td>
<td>local loads per thread</td>
</tr>
<tr>
<td></td>
<td>average cache lines per access per warp</td>
</tr>
<tr>
<td>Control Flow &amp;</td>
<td>barriers per thread</td>
</tr>
<tr>
<td>Synchronization</td>
<td>if statements per thread</td>
</tr>
<tr>
<td></td>
<td>for loop bodies executed per thread</td>
</tr>
</tbody>
</table>

Algorithm 1: Pseudo-code for counting the total number of loads/stores for each type of memory.

```
input :Lambda expression representing a program
output :Numbers of different types of memory accesses.
countAccesses(lambda)
1 totalLoad[local] = 0; totalLoad[global] = 0
2 totalStore[local] = 0; totalStore[global] = 0
3 countAccessesExpr(lambda.body, 1)
4 return [totalLoad, totalStore]

countAccessesExpr(expr, iterationCount)
5 switch expr do
6 case fc@FunCall
7   foreach arg in fc.args do
8     countAccessesExpr(arg, iterationCount)
9   switch expr / do
10  case is l@Lambda
11     countAccessesExpr(l.body, iterationCount) ;
12     case is l@Private or l@ToLocal or toGlobal
13     countAccessesExpr(t.f.body, iterationCount) ;
14     case is m@MapSeq or m@MapLcl or m@MapCld or ... 
15     n = fc.input(0).length
16     countAccessesExpr(m.body, iterationCount ^ n)
17     case is it@Iterate
18     countAccessesExpr(it.body, iterationCount ^ it.count);
19     case is u@UserFun
20     foreach arg in fc.args do
21       if totalLoad[arg.addressSpace] + it.iterationCount
22       totalStore[arg.addressSpace] += iterationCount
23     otherwise do // Nothing to count ;
24     otherwise do // Nothing to count ;
25     return counts

Example Consider the program in Listing 3. The algorithm starts with the top-level lambda and soon encounters the mapWrg primitive. At this point in the algorithm, line 14, n will be N/64 (the length of the outer dimension of the input after the split). The algorithm calls recursively countAccessesExpr with N/64 as the iterationCount. When visiting either of the mapLcl in line 3 of Listing 3, n will this time be 64 (the length of the inner dimension of the input after the split).

When the add function is visited, global loads is updated twice, since the add function has two inputs (the tuple is automatically unboxed). Since at this point, the iterationCount is N/64 = 64 = N, the total number of global loads is N + 2, and the total number of local stores is N. When the multByTwo function is visited, local reads and global store are both updated once, resulting in N local loads and N global stores.

4.2.3 Memory Access Patterns

The way a program accesses memory has a profound impact on performance. GPUs coalesce several memory requests into a single one when threads in the same warp/wavefront access a single cache line (typically 128 bytes). It is, therefore, important to extract information about memory access patterns for building an accurate performance predictor.

General Algorithm To determine the total number of cache line reads, our feature extractor recursively traverses the IR, keeping
track of the iteration count. When a memory access is encountered, it
determines the number of unique cache lines accessed by the
warp as follows. First, it generates the actual index expression using
the existing mechanism of the LifT compiler [35]. If the expression
contains no thread id, it means that all the threads are accessing
the same cache line.

When the expression contains a thread id, a new index expression
is generated for each thread in the warp by adding a constant to its
id (threads in a warp have consecutive ids). Let’s denote the original
array index expressed as a function of the thread id as \(access(tid)\).
Given \(n\), the number of threads in a warp, the set of array indices
accessed by the warp is:

\[
\{access(tid + 0), access(tid + 1), \cdots, access(tid + n - 1)\}
\]

This list of indices expresses the different addresses accessed by a
warp. Given the cache line size \(s\) (expressed as a multiple of data
size), we compute the list of cache lines accessed:

\[
\frac{access(tid + 0)}{s}, \frac{access(tid + 1)}{s}, \cdots, \frac{access(tid + n - 1)}{s}
\]

Finally, we can subtract the elements in the list with each other to
identify which ones are equal (when the subtraction results in 0)
and count the number of unique accesses.

Implementation details The approach explained above is con-
tursively correct, however, it relies on having the ability to symbol-
ically simplify arithmetic expressions. While the LifT arithmetic
simplifier supports a significant set of simplifications, it is not pow-
erful enough to deal with some simplifications. In such cases, the
feature extractor might fail to recognize identical accesses. The
following paragraphs explain a few workarounds used inside the
feature extractor.

The first issue we encountered, is the difficulty in calculating the
set of unique cache lines by subtraction. Conceptually, one could
take the first access \(access(tid + 0)/s\), subtract every other accesses
by it and hope that the algebraic simplifier would be able to return
0 in case where two accesses are identical. Simplifying expressions
as simple as

\[
\frac{(tid + 0)/s - (tid + 1)/s}
\]

which is 0 when \(s > 1\), is far from trivial given that \(\) represents
the integer division.

To overcome this challenge, we modify our approach slightly and
add an extra step. Before dividing by \(s\), we first calculate all the
relative array accesses as an offset of the first access by simple
subtraction. The intuition behind this is two-fold. First, it is much
easier to simplify a subtraction if it does not contain terms with
integer division. Second, we only care about the distances between
the accesses rather than their absolute location, therefore, we will
still be able to identify the number of unique cache line accessed.

So if the original accesses are

\[
\{tid + 0, tid + 1, \cdots\}
\]

they become

\[
\{(tid + 0) - (tid + 0), (tid + 1) - (tid + 0), \cdots\}
\]

which simplifies trivially to \(\{0, 1, \cdots\}\). Then, we perform the divi-
sion as before, which leads to \(\{0/s, 1/s, \cdots\\}\) which trivially sim-
pplies to \(\{0, 0, \cdots\}\). Now it is much easier to identify the unique
cache lines.

Example Consider the example program in Listing 4. The array
index being read for the argument of \(f\) is \(i + n \cdot gl_id\), where \(i\) is
the iteration variable of the mapSeq and \(gl_id\) the global thread id.
Depending on the split factor \(n\), a different number of cache lines
will be accessed by a warp. With a split factor of \(n = 1\), a single

\[
\text{Listing 4. Example for extracting memory access patterns.}
\]

\[
\text{Example (in: [float]n) = mapGlb(mapSeq(f), split(n, in))}
\]

control flow and synchronization.

Another important factor that often limits performance on GPUs
is control flow and synchronization. if-then-else and for loop state-
ments produce branching instructions which is notoriously bad
for GPU performance because they typically cause control flow
divergence within warps. Similarly, barriers are detrimental to per-
formance since execution is altered until all threads have reached
the barrier. For this reason, the feature extractor determines the
total number of if-then-else, for loops and barriers produced by the
code generator.

Algorithm This is similar to the algorithm used to count the num-
ber of memory operations. It traverses the IR recursively, keeping
track of the number of times each function is executed. Whenever a
pattern that might produce a loop (e.g. iterate, mapLocal, reduceSeq)
is encountered, it checks whether a loop will be emitted and update
a global loop counters, taking into account the current iteration
count.

The algorithm also detects special cases where loops might not be
emitted. There are two cases to consider. First, when a mapSeq
iterates over an array of size 1, it is clear that a loop is not required.
The second case is more subtle and involves mapLocal, mapWrg or
mapGlobal. If the size of the input array is smaller than the number
of local threads, workgroups or global threads, respectively, the code
generator will emit an if-then-else statement instead of a loop since
the loop can at most be executed once per thread or workgroup.

To determine the number of barriers, the algorithm looks at
mapLcl as OpenCL only has barriers inside workgroups. The LifT
Another practical issue has to do with the
high-level GPU-specific features are
extracted using information about the
length of arrays from the type. We have seen how the fine-grained
memory feature related to cache lines accesses is computed using
the power of the Lift symbolic arithmetic expressions. The next
section explains how we build a simple performance model using
these extracted features.

5 Performance Model

Having seen how hardware-specific information is extracted from
the high-level IR, we now focus on the performance model. It is
based on k-Nearest Neighbors (kNN), which makes prediction based
on the distance between programs in the feature space. Intuitively,
Lift programs that exhibit similar features are likely to have similar
performance.

5.1 Output Variable

The prediction output is throughput normalized by the maximum
achievable per input/program. This is to ensure that performance is
comparable across programs, since different programs might
exhibit different numbers of operations.

5.2 Principal Component Analysis

Given that a kNN model works best with a small number of features, we use PCA (Principal Component Analysis) to reduce the
dimensionality of the feature space. Prior to applying PCA, the
features are centered and reduced with a mean of 0 and a standard
deviation of 1. This step is necessary since our features have very
different ranges of values. PCA is then applied and we retain the
principal components that explain 95% of the variance. In effect,
this compresses the feature space by removing redundant features.

5.3 K-Nearest Neighbors Model

A k-nearest neighbors model makes a prediction of a new data
point by finding the k closest points to it, using Euclidean distance and averaging their responses to make a prediction. In our case,
the distance metric is determined by how close the feature vectors
are from one another.

The kNN model does not require any special training. The execution
time of rewritten Lift expressions, together with their features,
are simply collected and added into a database. When predicting a
newly unseen Lift program, we simply look up the k closest
neighbors and average their prediction to form a new prediction.
In our experiment, we used $k = 5$.

5.4 Making Predictions

To make a prediction about new programs, we first collect data
points from a group of training programs. For each program, we
conduct an exploration of their optimization space and store the
features and corresponding performance. Given a new program,
we proceed as follows:

1. For each rewritten program:
   a. The features are extracted, normalized and projected based
      on the PCA calculated from the training data;
   b. The model predicts the performance using the average of
      the k-nearest neighbors.

2. The different rewritten programs are sorted based on the
   prediction.

3. The fastest predicted rewritten program is generated, com-
   piled and executed.

6 Experimental Setup

Platform The setup consists of two GPUs, an NVIDIA Titan Black
and an AMD Radeon R9 295X2. The Nvidia platform uses driver
version 367.35 and OpenCL 1.2 (CUDA 8.0.0). The AMD platform
uses OpenCL 2.0 AMD-APP (1598.5).

Benchmarks and Space We use the 2D stencil benchmarks from
[9] listed in Table 2. All experiments are performed using single
floating point with matrix sizes from $512^2$ to $8192^2$.

Model evaluation The performance model is evaluated using
leave-one-out cross-validation, the standard machine learning method-
ology. When evaluating performance on a given benchmark, the
training data consists of all the data collected from all benchmarks,
except the one being tested.
7 Feature and Model Analysis

Before looking at how the performance model is used to speedup the optimization space exploration, we first perform an analysis of the features and evaluate the model accuracy.

7.1 Features Analysis

We use the redundancy metric to analyze which features are the most informative about performance:

$$R = \frac{I(X, Y)}{H(X) + H(Y)}$$

The redundancy metric normalizes the mutual information by the sum of the entropy of the two variables. This ensures that different features can be compared with one another. In our case, we are interested in comparing each feature with the output we wish to predict: performance. A higher value between a certain feature and the output indicates that the feature is useful for performance prediction.

Figure 4 shows the normalized mutual information between features and performance. As expected, one of the most important features is the average number of cache lines accessed per warp. This feature, which represents locality, is extremely important for stencil benchmarks.

The next most important feature for both machines is the global-Size in dimension 1. This feature is directly related to the number of threads that execute and, therefore, the amount of parallel work performed. It is also used to determine if the kernels are launched using a 2D or 1D iteration space (in the 1D case, the globalSize1 will be 1). Then, comes the number of global stores, followed closely by the number of global loads. This basically corresponds to the number of memory accesses performed into the slow global memory.

For both platforms, barriers and control flow (for loops) seem to have only a medium impact on performance, whereas the number of if-statements does not seem very relevant at all. Focusing on the least important features, the number of local loads does not seem to affect performance much. We conjecture that, since local memory is very fast, having fewer or more local loads might not make much of a difference in terms of performance, especially compared to the number of global memory operations.

7.2 Benchmark diversity

Figure 3 shows the features of the best point in the space for our benchmarks. As can be seen, some benchmarks share similarities, which is essential for being able to make prediction. However, we also observe quite a lot of diversity.
for Nvidia and 240 for AMD. These results clearly show that the performance model is working well in the majority of cases.

Interestingly, there are a couple of outliers programs/input size combination that require over 30 runs for the model-based approach. In both cases, stencil2d on Nvidia and srad1 on AMD, this is when the largest or smallest input sizes are used. We believe that in such cases, the behavior of these programs probably changes drastically with the input size. For instance, the data might actually fit entirely in the cache for the smallest input size of stencil2d and, therefore, change drastically the behavior of the application for this input size. Since our features have no notion of working-set size, the model might be unable to pick up this change of behavior. However, even in such cases, the model-based exploration is still ahead of random. For stencil2d, the model needs 31 runs while random needs 691, a 21x speedup!

9 Related Work

Auto-Tuning OpenTuner [1] is a framework for domain-specific multi-objective auto-tuners. CLTune [25] is a generic auto-tuner for OpenCL kernels. ATF [31] is a language-independent auto-tuning framework which supports inter-parameter constraints. These auto-tuning approaches attempt to find good implementations using online search which is orthogonal to our approach. In fact, auto-tuners can be easily coupled with a performance predictor.

Analytical Performance Modelling CuMAPz [16] is a compile time analysis tool that helps programmers increase the memory performance of CUDA programs. It estimates the effects of performance-critical memory behaviors, such as data reuse, coalesced accesses, channel skew, bank conflict and branch divergence. GROPHECY [23] uses the MWP-CWP model [12] (Memory Warp Parallelism – Computation Warp Parallelism) to estimate the GPU performance of skeleton-based applications. GPUPerf [33] is an enhanced version of the analytical MWP-CWP model with added metrics and a way of understanding performance bottlenecks. The boat hull model [26] is a modified version of the roofline model based on an algorithm classification and produces a roofline model for each class of device.

GPU cache models [27] have been built by extending reuse distance theory with parallel execution, memory latency, limited associativity, miss-status holding-registers and warp divergence. COMPASS [18] introduces a language for creating analytical performance models that analyze the amount of floating point and memory operations based on static code features. Coloured petri nets [20] were proposed for GPGPU performance modeling. Another approach [3] builds an analytical performance model to determine the lower bound on execution time. Low-level GPU ISA solving and assembly microbenchmarking [38] has been used to collect data about architectural features and performance.

Sensitivity Analysis via Abstract Kernel Emulation [11] aims to predict execution time and determine resource bottlenecks for a given Nvidia GPU kernel binary. Analytical models describe low-level details of the hardware to model performance using a model written by a hardware expert. They typically use low-level kernel representations to make their predictions. In contrast, our approach based on machine-learning is fully automatic and works by extracting features at a much higher level.

Statistical Performance Modelling Early work [8] extracts static code features and uses machine learning to predict the performance of optimization sequences. Principal component analysis, cluster analysis and regression modelling have been used [15] to generate predictive models for GPUs and CPUs. Predictive modelling has also been applied in polyhedral compilation [29] to predict speedups for different combinations of polyhedral transformations from hardware performance counters. Graph-based program characterization [28] has also been used for polyhedral compilation to predict the speedups of optimization sequences. Clustering on similarity of a graph-based intermediate representation has been used [7] to cluster similar programs. Another approach [36] uses machine learning models trained on assembly-level features to choose a good combination of transformations for vectorization.

Figure 3. Radar plot of the features for the top points in the space (input sizes 4K).

Figure 4. Normalized mutual information (redundancy) between each feature and performance.
All these approaches use hardware counters, low-level code features, assembly-level features or compiler data structures to predict speedups or optimization sequences. In contrast, our work shows how we can extract features at a much higher level and still predict performance accurately.


These approaches try to directly predict the effect tunable parameters have on the performance. However, they rely on the fact that the number of parameters is fixed and known in advance. In contrast, our approach predicts the performance independently of the number of parameters in the program.

**Artificial Intelligence for Compilers** Genetic programming has been used [17] to generate features for predicting loop unrolling factors. Others [24] have proposed ways of generating program features out of simple ones. Features are encoded as numeric relations and new ones are generated by joining existing relations and aggregating them. TVM [5] uses machine learning to prune the search space for compilation optimizations.

Support Vector Machines have also been used in compilers [32]. Machine learning has also been used to automatically learn compiler heuristics. [37] A neural-network cascade [21] is used to determine the amount of thread coarsening to apply to OpenCL programs for different GPUs.

Machine learning models in compilers traditionally use features extracted from a deeper stage in the compilation pipeline. Our work instead extracts them at a considerably higher-level from a functional IR.

**10 Conclusions**

This paper has demonstrated that it is possible to extract low-level hardware-specific features from the Lift high-level functional IR. We have shown how type information, such as array length, is useful for computing certain features. The ability to reason symbollically about array indices also enables the extraction of very fined-grained features such as the number of accessed cache lines per warp. To the best of our knowledge, this is the first time a paper has shown how low-level features can be extracted at such high level, without requiring any profiling or performance counters.

The paper has also demonstrated how a simple performance model is built to make accurate performance predictions about different program variants. Using an Nvidia and AMD GPU, and stencil applications, we have shown that our model is able to predict points in the search space that are within 90% of the best within one or two runs in the majority of the cases. When compared to a random search strategy, the model requires on average 77x less runs than random on AMD and 35x less on Nvidia, which translates to time savings of 2000x and 450x respectively.